A versatile digital frequency synthesizer for state-dependent transport of trapped neutral atoms

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I hereby declare that this thesis was formulated by myself and that no sources or tools other than those cited were used.

Bonn, ...
Date Signature

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Abstract

This thesis deals with the design and construction of a versatile digital frequency synthesizer for implementation in the state-dependent transport of Cesium atoms. The versatile digital frequency synthesizer consists of a field programmable gate array interfaced with a low noise direct digital synthesizer that will be used for amplitude, phase and frequency modulation. The versatile digital frequency synthesizer provides better flexibility, for generating arbitrary waveforms, and lower phase noise than the previous setup. The measured reduction in phase noise of around 20dB corresponds to an increase in the lifetime of atoms by two orders of magnitude. This improved phase noise specification with the ability to generate arbitrary waveforms opens up possibilities for transporting atoms over macroscopic distances and eventually realizing an atom interferometer with a large space-time area.

1

Introduction

The invention of the laser in 1960 opened up new avenues in the field of atomic physics, eventually giving rise to the field of quantum optics. Not only were lasers a good source of monochromatic light for probing atomic structures, but they have been used since the late 1970s to control the motion of atoms [1]. Laser cooling atoms down to very low temperatures provided a major boost to the field of precision spectroscopy and paved way for the experimental realization of fascinating new effects with ultracold gases, such as Bose-Einstein Condensation [2–4].

Quantum optics also deals in large part with the manipulation of single atoms, providing experimental evidence for thought experiments about the quantum nature of particles and furthering our understanding of the microscopic world in general. In particular, optical lattices offer precise control of atoms in periodic potentials, which makes them an ideal choice for quantum simulators [5, 6]. Furthermore, such spatial control also opens up the possibility to conduct interesting experiments such as controlled interactions between atoms to produce ultracold molecules [7], creation of large scale entanglement and realization of fundamental quantum gates on cold atoms [8]. A promising experimental approach to letting atoms interact in a controllable way is based on the deterministic transport of atoms, which is typically realized by trapping atoms in dipole potentials created by the optical lattices and transporting them by detuning the frequency between the two counter-propagating waves [9, 10].

A higher degree of control is achieved in the state-dependent transport scheme implemented in our group in Bonn where the internal state of the cesium atom is coupled to its spatial degree of freedom. This gives us the ability to independently control the motion of atoms which are in different internal states, represented by $|\uparrow\rangle$ and $|\downarrow\rangle$. State-dependent transport of cesium atoms has been employed in many interesting experiments, such as the implementation of quantum walks [11] and the realization of a single atom interferometer [12].

1.1 Motivation: Long distance atom interferometers

Atom interferometry exploits the wave nature of atoms in order to create interference effects analogous to optical interferometry. Initially used to demonstrate the principles of quantum mechanics, atom interferometers now lie at the heart of precision measurements.

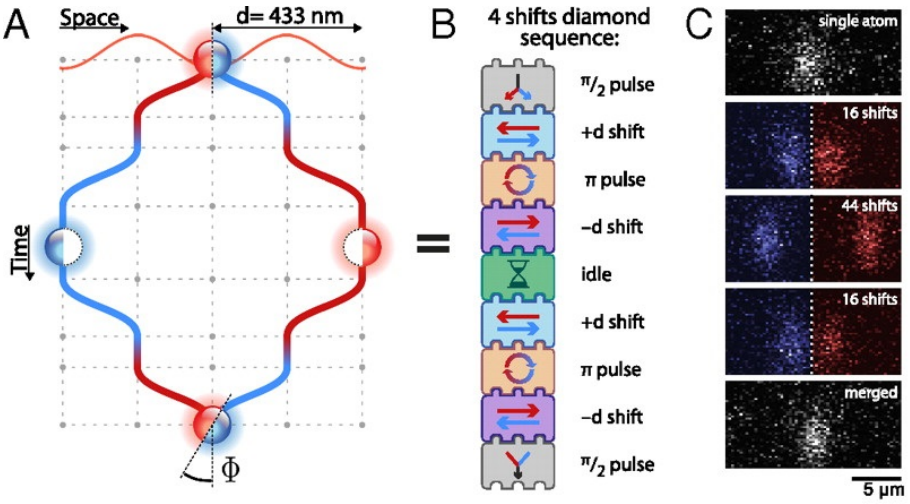

Figure 1.1: Digital atom interferometer. (A) A spin dependent optical lattice coherently transports the atom depending on its spin state, $|\uparrow\rangle$ (red) or $|\downarrow\rangle$ (blue), in opposite directions and finally recombines the two states, creating a diamond interferometric geometry. (B) Digital block representations of the operations mentioned in A. (C) Fluorescence images of atoms illustrate the splitting achieved. Figure taken from [12]

They have been used for precision measurements of gravity acceleration [13], gravity gradients [14], the fine structure constant [15], Newton's gravitational constant [16, 17] and for other applications in geophysics. Atom interferometers can be based on different conceptual schemes including the Mach Zehnder [18], Talbot-Lau [19], Ramsey-Bordé [20], and stimulated Raman transition interferometers [21]. While some atom interferometers render interference patterns in position space, others render them in momentum space or even in internal state space. For a measurement of small rotations, compared to optical interferometers, an atomic interferometer of equivalent area has the possibility to make 10^{11} times more precise measurements [22]. Furthermore, they can be used to probe a wider variety of physical phenomena by virtue of their mass. Even compared to electron and neutron interferometry, atom interferometers have many advantages. They offer a wider range of atomic properties, a larger cross-section, better characterized interaction with the environment and higher precision [21]. For instance the mass of a cesium atom is 137 times that of hydrogen, making it better suited to measure inertial effects.

While most atom interferometers work with an ensemble of atoms that propagate freely through space, we realized a trapped single atom interferometer with deterministic transport of the two arms of the interferometer. There are two primary advantages of using a trapped single atom interferometer. Firstly, the wave-function is highly localized in space, allowing us, in principle, to measure local forces such as the Casimir-Polder force. The second advantage is the spatial control over the two spin states of the atom, which constitute the two arms of the interferometer, allowing us to design any complex interferometric geometry that can improve the sensitivity of the interferometer [12]. Figure 1.1(A) shows a diamond geometry that was implemented in the experiment using operations represented as digital blocks in (B).

An atom is split in a spin-state superposition using the state preparation and manipulation technique, explained in section 2.1. The two spin components, $|\uparrow\rangle$ and $|\downarrow\rangle$, are coherently transported depending on their spin state and eventually recombined to extract the phase difference Φ accumulated between them. This phase was extracted by means of a Ramsey probing scheme, where the phase information was mapped onto the two spin populations [12]. At the time of this experiment, the maximum shift possible in one operation was half a lattice site for each spin state. Hence, the shift operations were interleaved with spin flip operations in order to increase the distance between the arms of the interferometer.

The phase acquired by the interferometer in the presence of a linear potential gradient is proportional to the space-time area enclosed between the two paths. Hence, to improve the precision of the measurement, it is desirable to increase it. While increasing the distance traversed by the two arms is the obvious choice for any interferometer, a trapped atom interferometer provides an additional option of increasing the time that the two arms are allowed to evolve over. This is shown in fig 1.1, where an idle block (pause in transport) is implemented when the two arms are furthest apart. The coherent separation reached between the two spin states in the experiment was around $10\mu m$ and the coherence time, enhanced by spin-echo techniques, was of the order of 2.3ms [12].

The motivation for undertaking this thesis work is to build a versatile digital frequency synthesizer, an integral component in the experiment used for precise transport of atoms, that will help improve the transport fidelity and coherence times of the atoms in order to achieve a long distance atom interferometer. Splitting the wavefunction on the order of 1 mm coupled with long coherent times will help increase the space-time area enclosed by a factor of 10^5 [12], thereby putting us on par free-fall atom interferometers.

Outline

With the general scheme of the digital atom interferometer laid out in the preceding section, in chapter two I will discuss the underlying concept behind the state dependent transport scheme and its experimental realization. The latter half of the chapter lists out the current limitations to achieving a long distance single atom interferometer.

Chapter three will discuss the versatile digital frequency synthesizer in more detail. Chapter four discusses phase noise measurements of the versatile digital frequency synthesizer and finally in chapter five I sum up the work done during the thesis and give a glimpse of novel experiments that can be performed after installing the versatile digital frequency synthesizer in the experiment.

2

State-dependent transport

The preceding chapter illustrated an application of the state-dependent technique for realizing a atom interferometer. In this chapter I will briefly present the state-dependent transport scheme whereas further information can be found in [23–27]

2.1 Preparation of qubit states

A prerequisite for state-dependent transport is the control over the internal quantum states of the atom. We select the outermost Zeeman sublevels of the two hyperfine manifolds of the cesium ground state as our spin $|\uparrow\rangle$ and spin $|\downarrow\rangle$ states, as shown in figure 2.1. The atom is prepared in state $|\uparrow\rangle$ by means of optical pumping, where a σ^+-polarized pump laser beam is set at the $|F = 4\rangle \rightarrow |F' = 4\rangle$ transition and a σ^+-polarized repumping beam is set at the transition $|F = 3\rangle \rightarrow |F' = 4\rangle$. An advantage of choosing the outermost sub-levels of the atom as our two states is that the state $|\uparrow\rangle$ is a dark state. This means that once the atom has decayed into this state from the $|F' = 4\rangle$ state, it is effectively transparent to the σ^+ polarized pumping laser beam and hence the atom

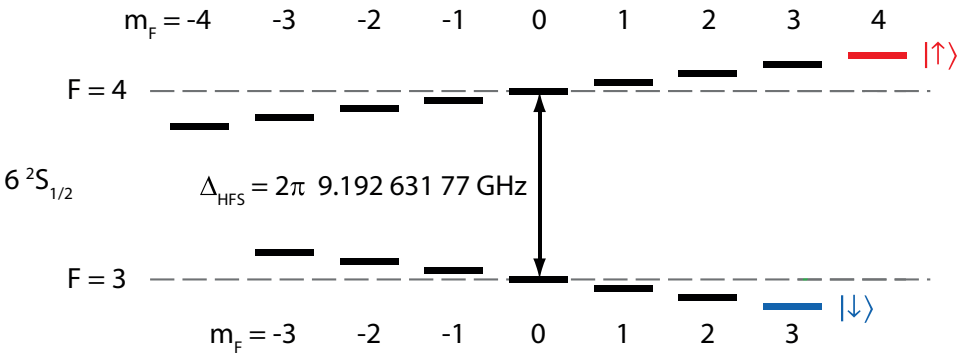

Figure 2.1: A magnetic field is applied to Zeeman shift the magnetic sublevels of the hyperfine manifold of the ground state. The degeneracy of the Zeeman sublevels is lifted by applying a magnetic field such that the transition frequency between the two levels is sufficiently far away from the other transition frequencies. The outermost sublevels are chosen as the two states of the effective two level system with pseudospin $|\uparrow\rangle = |F = 4, m_F = 4\rangle$ and $|\downarrow\rangle = |F = 3, m_F = 3\rangle$.Figure taken from [26]

remains prepared in this state for a long time. Once prepared in the $|\uparrow\rangle$ state, the atom can be driven to the $|\downarrow\rangle$ state or to a superposition of the two qubit states by applying a microwave radiating at a frequency of 9.2 GHz.

The geometrical representation of the pure state space of such a two level system can be visualized on a Bloch sphere—a unit sphere in $\mathbb{R}^3$, giving a geometrical representation of the qubit state. The north and south poles of the Bloch sphere correspond to $|\uparrow\rangle$ and $|\downarrow\rangle$ states respectively, as shown in figure 2.2. Any generalized qubit state in a two level system $|\psi\rangle = \alpha\,|\uparrow\rangle + \beta\,|\downarrow\rangle$ corresponds to a radial vector on the Bloch sphere with its tip on the surface of the sphere. In the polar coordinate system, this vector can be represented as

$$|\psi\rangle = \cos(\theta/2)\,|\uparrow\rangle + \mathrm{e}^{i\phi}\sin(\theta/2)\,|\downarrow\rangle\,, \tag{2.1}$$

where $0 \leq \theta \leq \pi$ is the polar angle and $0 \leq \phi \leq 2\pi$ is the azimuthal angle. When driven by microwave radiation, the Bloch vector evolves in time as the magnetic moment interacts with the microwave field. This evolution can be approximated by the optical Bloch equations [28]. In cartesian coordinates, the Bloch vector is

$$\mathbf{u} \equiv (u, v, w) = (\cos\phi\sin\theta, \sin\phi\sin\theta, \cos\theta), \tag{2.2}$$

where positive u,v and w axes correspond to the states $\frac{1}{\sqrt{2}}(|\uparrow\rangle + |\downarrow\rangle)$, $\frac{1}{\sqrt{2}}(|\uparrow\rangle + i\,|\downarrow\rangle)$ and $|\uparrow\rangle$ respectively. Analogous to the Bloch equations used in nuclear magnetic resonance [29], a set of optical Bloch equations (also known as the Maxwell Bloch equations) describe the evolution of the Bloch vector in a two level system [30]. To calculate the evolution of the Bloch vector, we consider a microwave field described as

$$B_{\mathrm{MW}} = B_0\cos(\omega_{\mathrm{MW}}t + \phi_{\mathrm{MW}}), \tag{2.3}$$

where B_{MW} is the field strength, ω_{MW} the frequency and ϕ_{MW} the phase. The Bloch equations can then be written in a vectorial form as:

$$\dot{\boldsymbol{u}} = -\boldsymbol{\Omega} \times \boldsymbol{u}, \tag{2.4}$$

where $\boldsymbol{\Omega} = (\Omega_R\cos\phi_{\mathrm{MW}}, -\Omega_R\sin\phi_{\mathrm{MW}}, \delta)$ is the torque vector. $\Omega_R = \mu B_{\mathrm{MW}}/\hbar$ is the Rabi frequency with μ being the dipole moment and $\delta = \omega - \omega_0$ the detuning of the microwave frequency from the frequency of the $|\downarrow\rangle \rightarrow |\uparrow\rangle$ transition. Taking ϕ_{MW} to be zero, resonant microwave pulses($\delta = 0$) rotate the Bloch vector around the u axis, as shown in figure 2.2. The angle θ that the vector is rotated by is the time integral of the Rabi frequency Ω_R over the duration of the pulse.

$$\theta(t) = \int_0^t \Omega_R(t')dt' \tag{2.5}$$

Two prominent pulses used are the π-pulse ($\theta(t) = \pi$), corresponding to complete population transfer, and the $\pi/2$-pulse ($\theta(t) = \pi/2$), which corresponds to the creation of an equal superposition of states, as needed for the single atom interferometer. These two

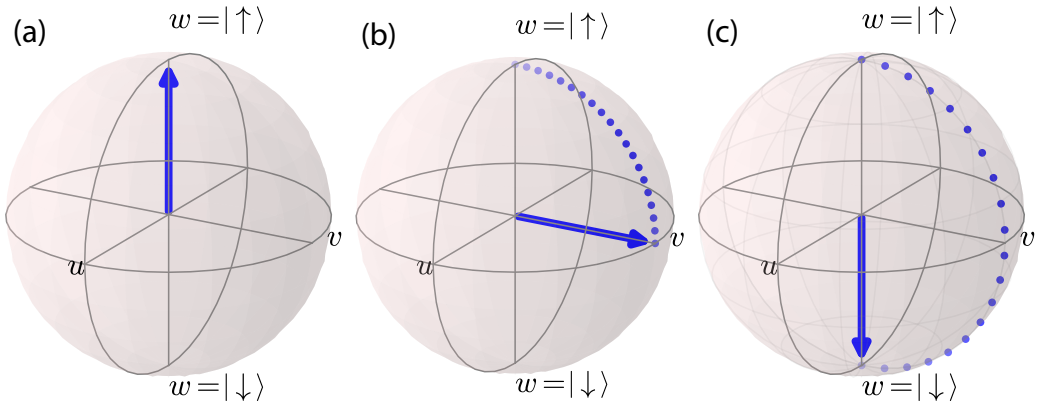

Figure 2.2: The atoms is prepared in state $|\uparrow\rangle$ in (a) given by (0,0,1). A resonant $\pi/2$-pulse rotates the vector to state $\frac{1}{\sqrt{2}}(|\uparrow\rangle + |\downarrow\rangle)$ in (b) which corresponds to (0,1,0). A resonant π-pulse applied to (a) drives the atom to $|\downarrow\rangle$ state, given by (0,0,-1). Figure taken from [26]

conditions have been shown in figure 2.2. By controlling the duration of the microwave pulse one can achieve different superposition states of $|\uparrow\rangle$ and $|\downarrow\rangle$.

2.2 State-dependent transport

To implement state-dependent transport for the two spin states, we need two dipole potentials for separately trapping the spin species. To better understand the creation of state dependent potentials, we consider the simplified fine structure representation of the cesium ground state $^2S_{1/2}$, as shown in figure 2.3.

In the fine structure representation, the two qubit states $|\uparrow\rangle$ and $|\downarrow\rangle$ are represented by their fine structure counterparts, namely

$$|\uparrow'\rangle = |J = 1/2, m_J = +1/2\rangle \qquad |\downarrow'\rangle = |J = 1/2, m_J = -1/2\rangle \tag{2.6}$$

In the presence of a light field, shifts in the energy levels are caused by the ac Stark shift. The shift in energy levels creates a dipole potential which, depending on the detuning of the light field, can either be attractive (red-detuned) or repulsive (blue-detuned). For the cesium ground state, light shifts are dominated by the contributions from the first two excited states $^2P_{1/2}$ and $^2P_{3/2}$. The transition from $^2S_{1/2}$ to $^2P_{1/2}$ and $^2P_{3/2}$ states are termed the D_1 and D_2 lines respectively and they are of wavelength $\lambda_{D_1} = 894.592$nm and $\lambda_{D_2} = 852.347$nm [31].

In order to use the first two excited states to create spin-selective potentials, a linearly polarized light field, that can be decomposed into a superposition of σ^+ and σ^- polarized light fields, is tuned to a frequency between the D_1 and D_2 lines. This light field is red-detuned to the $^2S_{1/2} \rightarrow {}^2P_{3/2}$ transition, creating an attractive potential, and blue-detuned to the $^2S_{1/2} \rightarrow {}^2P_{1/2}$ transition, creating a repulsive potential. For a particular wavelength of the light field, termed the "magic wavelength", the contribution from P

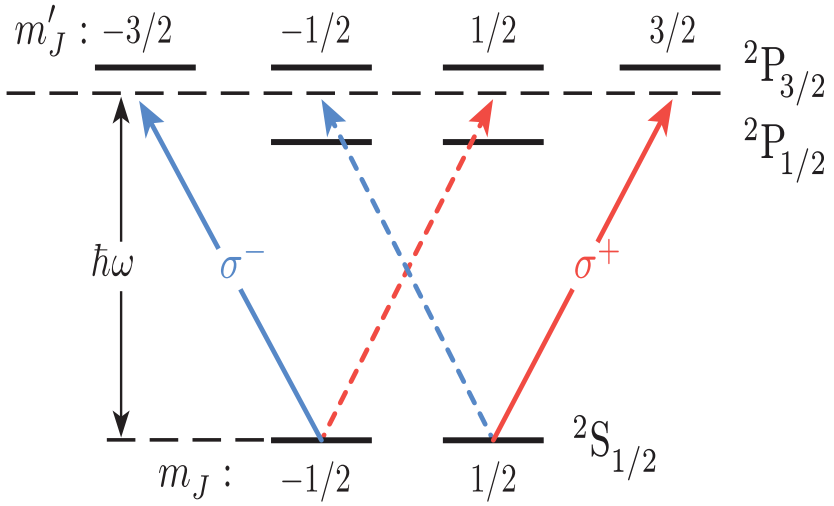

Figure 2.3: Fine structure representation of the cesium ground state. ω is the frequency of the laser between the D_1 and D_2 transitions for the case where the potential contributions from the $m_J = \pm 1/2$ magnetic sublevels of the two excited states cancel each other out.

states with $J = 3/2$ and $m_J = \pm 1/2$ is canceled by that of states with $J = 1/2$ and $m_J = \pm 1/2$. Hence the attractive potential contribution from the outermost states $m'_J = \pm 3/2$ of the $^2P_{3/2}$ level form the state-selective potentials. Atoms in the $m_J = +1/2$ ground state $|\uparrow'\rangle$ feel the attractive potential created by the σ^+ polarized component of the light field and atoms in the $m_J = -1/2$ ground state $|\downarrow'\rangle$ feel the attractive potential created by the σ^- component of the light field.

In reality, we have to consider the hyperfine levels of cesium in order to calculate the contribution of the σ^+ and σ^- polarized components to our initial qubit states $|\uparrow\rangle$ and $|\downarrow\rangle$. The qubit states $|\uparrow\rangle$ and $|\downarrow\rangle$ in terms of the fine structure basis states $|\uparrow'\rangle$ and $|\downarrow'\rangle$ are [23]

$$\begin{aligned} |\uparrow\rangle &= |I = 7/2, m_I = 7/2\rangle \otimes |\uparrow'\rangle \\ |\downarrow\rangle &= \sqrt{\frac{7}{8}}\Big(|I = 7/2, m_I = 7/2\rangle \otimes |\downarrow'\rangle \Big) + \sqrt{\frac{1}{8}}\Big(|I = 7/2, m_I = 5/2\rangle \otimes |\uparrow'\rangle \Big) \end{aligned} \tag{2.7}$$

We notice here that while the state $|\uparrow\rangle$ has a definite spin orientation, i.e., a defined m_J, the state $|\downarrow\rangle$ is an admixture of both states $|\uparrow'\rangle$ and $|\downarrow'\rangle$ with opposite m_J. The "magic wavelength" for this particular configuration is [23]

$$\lambda_{\text{magic}} = 865.9\text{nm} \ . \tag{2.8}$$

The quantization axis is defined by a magnetic field along the direction of the dipole laser beams forming the counter-propagating configuration. The resulting potential is

still periodic but with an amplitude for $|\downarrow\rangle$ that depends on the relative position [32]. The dipole potential can be decomposed into σ^+ and σ^- components given by

$$\begin{aligned} V_+(x,\phi) &= V_0 \cos^2(kx+\phi) \\ V_-(x,\phi) &= V_0 \cos^2(kx-\phi) \end{aligned} \tag{2.9}$$

where k is the wave-vector of the dipole laser, V_0 is the potential depth of the lattice and ϕ is the angle between the polarization vectors of the two counter-propagating waves. Changing this angle by $\Delta\phi$ corresponds to a shift between the potentials by

$$\Delta x = (\Delta\phi/2\pi)\lambda_x/2 \tag{2.10}$$

Hence, the distance between the two potentials can be independently adjusted by changing the optical phase of either the σ^+ or the σ^- component, resulting in the transport of either $|\uparrow\rangle$ or $|\downarrow\rangle$ respectively, as shown in figure 2.4. This is the principle used behind state-selective transport. The experimental realization of precise control over the phase of the two circularly polarized components will be discussed in section 2.4.

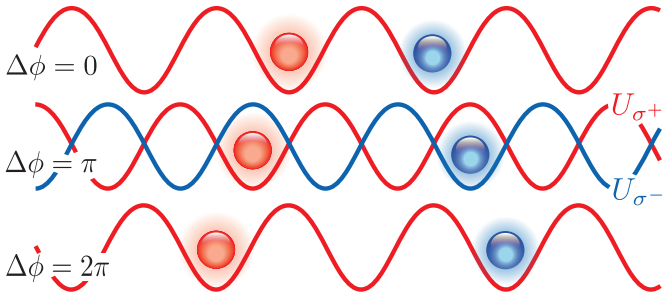

Figure 2.4: Illustration of state-dependent transport where the red-coloured (on the left-hand side) and blue-coloured (on the right-hand side) atoms constitute the two spin species of cesium. A 2π optical phase difference between the two circular polarizations corresponds to transport over one lattice site.

2.3 Experimental realization of state-dependent transport

This section gives a brief overview of the experimental setup and the experimental protocol for the state-dependent transport of neutral cesium atoms in a one-dimensional lattice. A detailed description of the experimental setup can be found in [23, 25, 33]

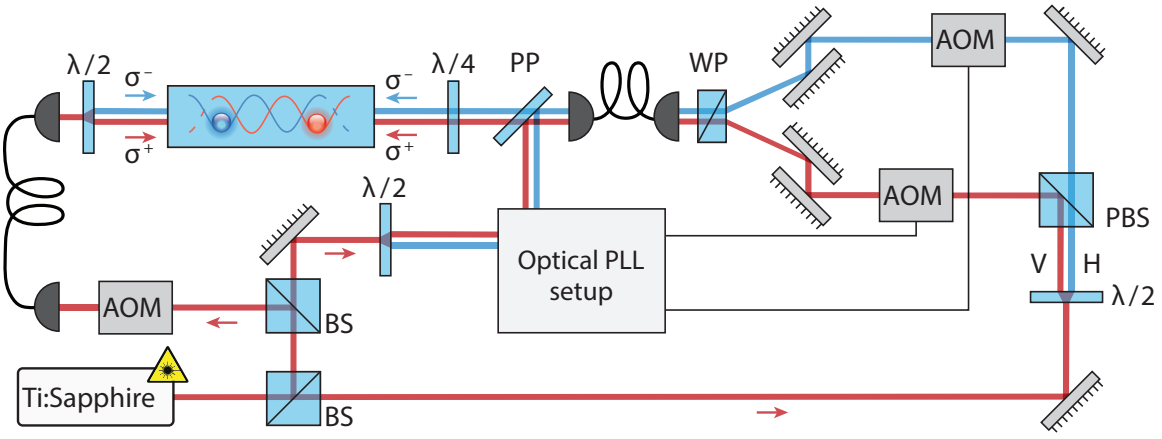

Figure 2.5: Schematic of the experimental setup. This sketch gives a simple overview of the beam paths and a few components of importance to this thesis. Several optical components needed for beam alignment are omitted, and so are the coils required to produce the magnetic fields. For a detailed sketch of the entire setup ,see [33].Figure taken from [33]

A schematic of the setup is shown in figure 2.5. The atoms are cooled and trapped in a magneto optical trap (MOT) which is a source of pre-cooled atoms for dipole traps. The MOT is overlapped with the dipole trap in an ultra-high vacuum cell of residual pressure smaller than 10^{10} mbar. Such low pressures are required to minimize collisions with atoms from the background gas that displace the atoms out of the trap. The MOT works on the principle of velocity dependent Doppler cooling and a position dependent restoring force created by a magnetic gradient [34–36]. The MOT laser[1] is set to the D_2 transition of Cesium at 852nm. Atoms in the MOT are cooled down to temperatures around 125μK. The radius of the cloud of trapped atoms, and hence the number of trapped atoms can be adjusted by tuning the strength of the magnetic field gradient. Once the atoms are trapped in the MOT, they are loaded into the dipole trap. The MOT beam intensity and frequency are adiabatically changed to molasses settings for imaging. Further details on the chain of events before transporting atoms can be found in [23]. Once the quantization axis has been set by applying a magnetic field along the lattice direction, the optical pumping (and repumping) beams are applied for state preparation, as discussed in section 2.1.

The laser beams entering the science chamber from both directions form the optical lattice (see fig 2.5). The beam entering from the left is directly sent through an acousto-optic modulator (AOM) after the laser source, while the beam entering from the right is synthesized from σ^+ and σ^- polarized beams. These two polarized laser beams create the two spin-dependent potentials. As shown on the right side of figure 2.5, the beam originating from the Ti-Sapphire laser[2] is sent through a polarizing beamsplitter (PBS) to separate the horizontal and vertical components of the polarization. These two orthogonal components are sent through AOMs which control their phase, frequency and amplitude.

[1] In-house-built interference-filter-stabilized external cavity diode laser
[2] Coherent MBR:110

The first order diffracted beams from the two AOMs are combined using a Wollaston prism and sent through a $\lambda/4$ plate to create an orthogonal pair of circularly polarized beams. The resulting polarization purity, corresponding to an extinction ratio after the Wollaston prism is around 10^{-4}.

The two orthogonal linearly polarized beams that go through the two AOMs have an interferometric geometry since they are split at the PBS and recombined again. Traveling through different paths, the two beams can acquire different phases due to external influences. This differential phase acquired manifests as a position fluctuation of the optical lattice. In order to compensate for this instability in position, a feedback loop is implemented.

2.4 Polarization synthesis

A schematic of the optical phase locked loop (OPLL) is shown in figure 2.6. Starting from the optical reference signal that enters from the left-hand side, I will follow the path taken by the beam, and describe the different components as they are encountered. The reference beam shown in the figure is directly sourced from the Ti-Sapphire laser (see figure 2.5). It is mixed with a small fraction of the dipole beam (consisting of the two circular polarizations) that is reflected off the mirror behind the science chamber. Mixing the optical reference signal with the reflected signal creates an optical beat signal which contains the phase and frequency information of the dipole trap beams with respect to the reference beam. This is the basic principle behind optical heterodyne detection. The beat signal oscillates at 80 MHz, since the dipole beam is 80 MHz frequency shifted by the AOM. This beat signal is sent through a Wollaston prism to separate the two orthogonal linear polarizations. We will consider the case of one circularly polarized component since the other goes through an analogous setup. The beat signal is detected by a fast photo-diode which produces a voltage signal corresponding to the 80 MHz beat signal. The voltage of the photo-diode is fed to a phase-frequency discriminator (PFD) where it is compared with an electronic reference signal, in our case a sinusoidal signal from a direct digital synthesizer (DDS)[3] running at 80MHz. The PFD compares the phase between the electronic reference signal and the signal from the photo-diode and outputs a DC voltage corresponding to the difference in the phase of the two. This voltage signal is sent to a proportionl-integral-derivative (PID) controller, which in turn sends out an actuating signal to the AOM driver. The AOM driver is a voltage controlled oscillator (VCO) which changes its oscillation frequency depending on the input voltage, in our case the actuating signal from the PID controller. A change in the frequency of the VCO leads to the change in frequency of the first order diffracted beam of the AOM. This first order diffracted beam from the AOM goes back to the science chamber, closing the feedback loop for phase stabilization. We are able to achieve a relative position stabilization of 60 pm using this feedback scheme.

To realize arbitrary transport sequences, we need to ideally be able to program arbitrary phase ramps of the RF reference signal provided by the DDS chips. The DDS is a

[3] Analog Devices AD9954

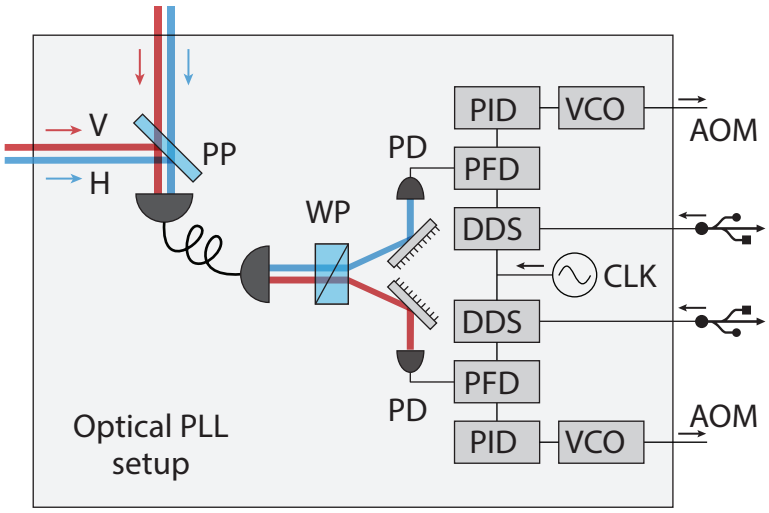

Figure 2.6: A simple schematic showing the basic components of the optical phase lock loop. Detailed working of the OPLL is explained in the text.Figure taken from [33]

digital device that can be programmed by the user. Transport of atoms in the optical lattice is achieved by changing the phase of the electronic reference, which is then imprinted onto the optical phase of the dipole beams through the feedback mechanism. As a key component of the transport scheme, the DDS has to meet the requirements of the experiment in terms of flexibility in modulating the phase of the electronic reference and in terms of phase stability.

2.4.1 Direct digital synthesis

Direct digital synthesis is a method of producing an analog waveform by generating a time-varying signal in digital form and then performing a digital to analog conversion. Figure 2.7 illustrates the functional blocks of the DDS.

A DDS uses a digital block to divide down the reference clock it receives, in order to generate the desired output frequency. The reference clock is shown in figure 2.7 as f_{clk}. The output frequency is set by sending a frequency tuning word (denoted by Δp in figure 2.7) to the frequency register of the phase accumulator. The phase accumulator consists of a j-bit frequency register, a j-bit adder and a j-bit phase register. At every clock edge of the reference clock f_{clk} (or $1/f_{clk}$ seconds), the j-bit value from the frequency register (which corresponds to the frequency tuning word, Δp) is added to the previously stored j-bit value of the phase register. A modulo-2^j value is sent from the phase accumulator to the phase to amplitude converter, which is usually a sine look-up table. The phase accumulator can be pictured as a phase wheel where going one circle around the wheel corresponds to stepping through one sine period. The j-bit phase wheel can be broken down into 2^j points where each point corresponds to a point on the sine wave. At every clock edge of the f_{clk}, Δp steps are added to the phase wheel, the result of which is sent to the look-up table. Since the number of steps on the phase wheel is 2^j, the output from

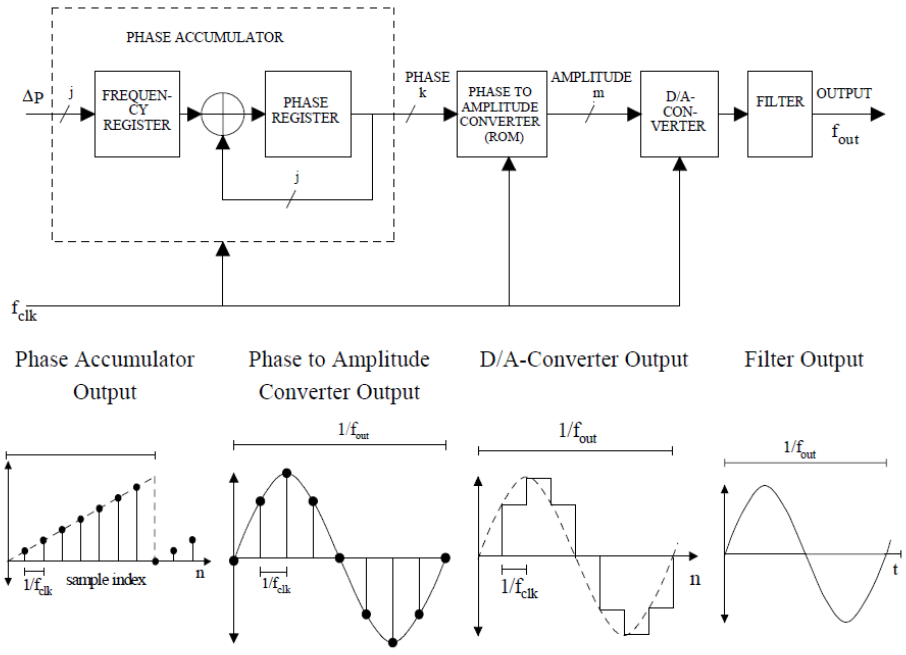

Figure 2.7: Block diagram of a direct digital synthesizer with the corresponding signal flow. Figure taken from [37]

the phase accumulator is always a modulo-2^j value. The output frequency is given as

$$f_{out} = \frac{\Delta p \cdot f_{clk}}{2^j} \tag{2.11}$$

and the frequency resolution of the DDS is

$$\Delta f = \frac{f_{clk}}{2^j} \ . \tag{2.12}$$

The look-up table converts the phase point it receives to an amplitude point, as shown in figure 2.7. This digital signal is then fed to a digital to analog convertor (DAC). The output of the DAC contains high frequency sampling components which are removed with the help of a filter in order to output a clean sine wave of the desired frequency. In order to generate a fixed frequency at the output, the tuning word sent to the phase accumulator is fixed. In addition to this, the DDS offers the capability to add a k-bit phase offset word to the frequency being generated. This offset is added before the look-up table and gives the capability to modulate the phase of the output signal. The phase resolution of the DDS is

$$\Delta\phi = \frac{2\pi}{2^k} \ . \tag{2.13}$$

In the state-dependent transport experiment, the phase offset word of the DDS is used for changing the phase of the electronic reference. The direct digital synthesizer has various

advantages over analog synthesizers, some of which are [38]

1. Lower phase noise. The phase noise of a DDS is lower than that of its reference clock while analog PLL-based synthesizers multiply the phase noise present in their frequency reference.

2. Micro-hertz frequency control and sub-degree phase tuning capability, all under complete digital control.

3. Extremely fast switching ($\sim$6 ns) between different phases and frequencies without any analog related loop settling-time anomalies.

4. Eliminates the need for manual system tweaking associated with analog synthesizers due to temperature drifts.

5. The system can be remotely controlled and minutely optimized.

Apart from the aforementioned advantages digital synthesizers are used in our experiment because as digital devices they can be programmed to perform arbitrary phase ramps (corresponding to arbitrarily shaped transport ramps) and any phase modulation performed is exactly reproducible. Although direct digital synthesizers have lower phase noise that analog synthesizers, there is still some phase noise contribution from its components and the reference clock which is imprinted onto the lattice beams. This phase noise manifests itself as position fluctuation of the lattice and it can lead to motional excitation of the atom, as discussed in the following section.

2.5 Effects of phase noise induced lattice fluctuations

Atoms in far off resonant optical traps have long lifetimes due to reduced spontaneous scattering rates [39]. In such traps, the lifetime is generally limited by other heating mechanisms such as laser intensity fluctuations or pointing instabilities of the laser [40] and ultimately by background pressure. Pointing instability has four major causes: thermal fluctuations, acoustic vibrations, mechanical vibrations and air convection [41]. Thermal drifts can lead to changes in the properties of optics used hence causing low frequency fluctuations of the lattice. Acoustic and mechanical vibrations can shake the optics used in the experiment, resulting in lattice fluctuations. Furthermore, air convection can lead to optical perturbations due to fluctuations in the density of air or scattering off dust particles.

As has been shown in [42], the lifetime of atoms in our experiment is not limited by the above mentioned causes but is instead limited by the relative phase noise $\Delta\phi$ between the AOM drivers used for the dipole trap which leads to heating of atoms until they are expelled from the optical dipole trap. This phase noise imprints itself onto the laser beam which leads to fluctuation of the dipole trap along the dipole trap [42]. The position fluctuation ϵ_x of the dipole potential is related to the relative phase noise as

$$\langle {\epsilon_x}^2 \rangle = \langle \Delta\phi^2 \rangle / k^2 \tag{2.14}$$

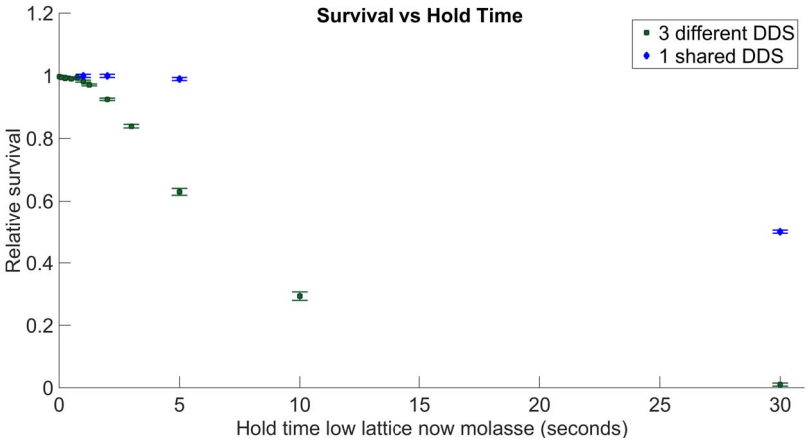

Figure 2.8: The relative survival of atoms for different hold times in two configurations. Data points shown as □ correspond to the case where all three DDS boards are used while in ◊ is the case where one DDS output is split into three instead. A significant increase in the survival time is noticeable when the lattice originates from the same RF source.

where k is the wave-vector along the dipole axis [42]. Currently, the differential phase noise between the two DDS boards limits the lifetime as well as the coherence times of the atoms. Long coherence times are crucial for achieving large separations with the atomic interferometer.

In order to confirm that this is the limiting case, instead of using the three boards for the three AOMs, the output of one board was split and used as the electronic reference signal [33]. This work was performed by Carsten Robens, a doctoral student in our group, and the difference between using three independent DDS boards and using one DDS board for all three AOMs is shown in figure 2.8. The lifetime of the atom in the dark, given in terms of the time after which the population drops to half, is around 5 seconds when three DDS boards are used. When one DDS board was used to drive the three AOMs, the lifetime increased to around 30 seconds. This clearly shows the effects of relative phase noise of the DDS boards on the lifetime of atoms. The heating rates of atoms in the trap are measured when the atom is in the dark since imaging of the atoms is done by the molasses beams which further cool the atom down, hence increasing their lifetime in the trap. Measuring the heating rate of atoms in a dark is used as a method to characterize the relative phase noise of the DDS boards.

Following the description in [40], [43] and [42] I will show the phase noise related heating in our setup. To understand the heating effects of lattice fluctuations in our setup, we consider a simple model of an atom in a one-dimensional harmonic potential well. This is given by

$$H = \frac{p^2}{2M} + \frac{1}{2}M\omega_x^2 x^2 \ , \tag{2.15}$$

where M is the mass of the atom, p the momentum and $\omega_x^2 (= k_x/M)$ the mean squared trap oscillation frequency along the dipole axis, k_x being the spring constant. Now we introduce a perturbing term in the Hamiltonian to represent the lattice fluctuations. The

new effective Hamiltonian is given by [43]:

$$H = \frac{p^2}{2M} + \frac{1}{2}M\omega_x^2(x + \epsilon_x(t))^2 \ , \tag{2.16}$$

where $\epsilon_x(t)$ is the time dependent fluctuation of the trap center. The perturbation of interest here is

$$H' = M\omega_x^2\epsilon_x(t)x \ . \tag{2.17}$$

Hence the average rate for an atom in state $|n\rangle$ at time t=0 to make a transition to the $|m \neq n\rangle$ in time T is given by Fermi's golden rule

$$R_{n\to m} = \frac{1}{T}\left|\frac{-\imath}{\hbar}\int_0^T dt' H'_{mn}(t')e^{\imath\omega_{mn}t'}\right|^2 \ . \tag{2.18}$$

Evaluating equation 2.18, it has been shown that the heating rate of atoms due to trap center fluctuations is given by [43]

$$\langle \dot{E}_x \rangle = \frac{\pi}{2}M\omega_x^4 S_x(\omega_x) \ . \tag{2.19}$$

Here $S_x(w)$ is the one sided power spectrum for trap fluctuations in the center and it is defined such that

$$\int_0^\infty S_x(\omega)d\omega = \epsilon_x^2 \ , \tag{2.20}$$

where ϵ_x^2 is the mean square fluctuation in the trap center as given in eqaution 2.14.

2.6 Current limitations to the acieve a long distance interferometer

Two important requirements for a long distance interferometer are long coherent splitting of the atomic wave-function and long coherence times. We are primarily limited by the DDS in achieving a large space-time area for our interferometer [44]. The DDS used hitherto in experiments, e.g. in [45], is the AD9954 produced by Analog devices Inc.

Transport fidelity

Transport fidelity gives the rate of success in deterministically transporting an atom to a desired lattice site. If the fidelity of a sequence is given by f, then the total fidelity by the end of n such sequences is f^n. Hence for complex interferometric geometries where sequences are applied multiple times, it is important that the fidelities are extremely high. Transport fidelity drops because the atom trapped in the dipole potential undergoes motional excitation and is eventually heated out of the trap.

One contribution to a decreasing transport fidelity as the transport distance is increased comes from the electronic reference generated by the DDS chip. To change the phase of

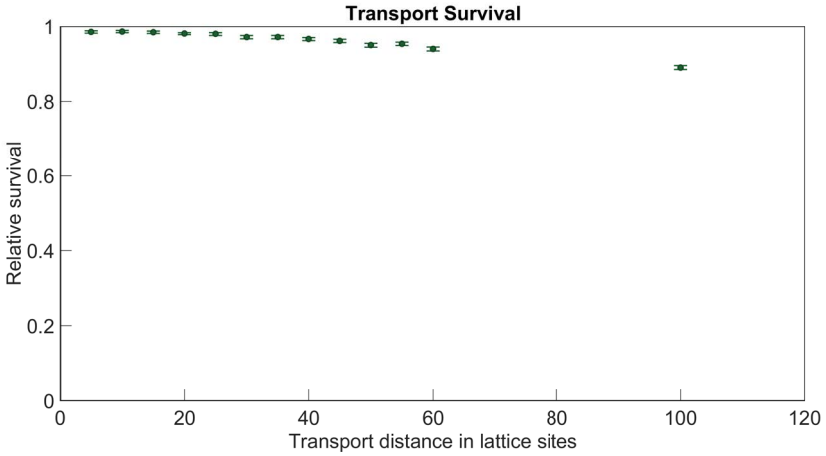

Figure 2.9: Transport survival for different transport distances. The survival probability drops as the transport distance is incresed.

the DDS output, a 14-bit phase offset word is sent to the DDS chip [46]. The AD9954 chip is limited to store 1000 of such phase offset words which are shared by 4 transport ramps. As the transport distance is increased, the lattice phase becomes more discrete since the phase discretization of the DDS is imprinted on the lattice beams. This discrete nature of the ramp is felt by the atom. This can either cause the atom to heat out or in extreme cases cause it to tunnel through the potential well. Figure 2.9 shows transport survival measurements performed by Carsten Robens [33]. Around ten percent of the atoms are lost when transported over a hundred lattice sites. In order to achieve better transport fidelity for longer distances it is necessary to replace the AD9954 DDS with a frequency synthesizer that can generate smooth ramps even for long transport distances.

Decoherence

It is essential that the superposition states used in the interferometer are maintained and that they do not lose their coherence. Decoherence mechanisms in our setup are studied in detail in ref. [47]. I will briefly mention a few causes of decoherence studied in [47] which are primarily limited by the AD9954 DDS chip. These causes of decoherence are closely related to the limitations in transport fidelity. One reason for which superposition states lose coherence is due to differential potential wobbling. As shown in equation 2.7, the $|\downarrow\rangle$ state feels a 1/8 contribution from the σ^+ light. Hence, there is a relative differential light shift experienced by the two spin components when they are being shifted [47]. This means that the two spin components acquire different phase and amplitude leading to a smaller overlap when they are recombined. This effect can be minimized by optimizing the transport ramp using optimal control. Here again, the limited number of phase points of the DDS limits our ability to implement optimized ramps for long transport distances. Another reason for decoherence is the relative fluctuation of the two lattices for the different spin states. As shown previously in section 2.5, this relative fluctuation of the lattice stems from the phase noise of electronic reference signal.

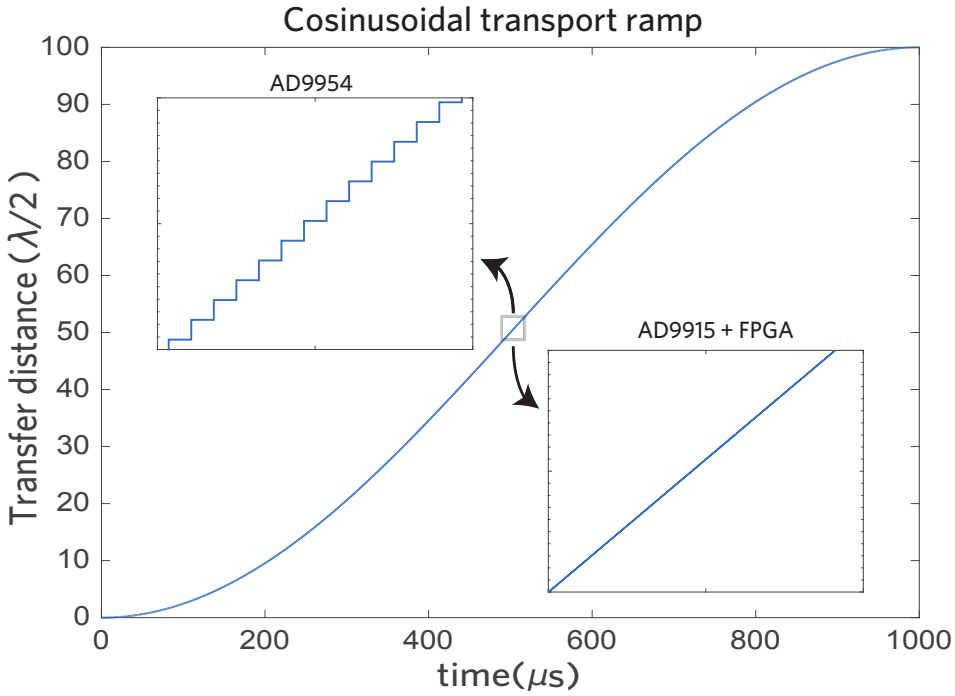

Figure 2.10: Phase ramp for transport over 100 lattice sites. Comaprison of the AD9954 DDS chip with the versatile digital frequency synthesizer (AD9915+FPGA).

From the limiting factors discussed above, we can infer that it is necessary to change the current electronic reference source, AD9954, in order realize a long distance atom interferometer. It is the objective of my master's thesis to develop a new digital synthesizer overcoming these limitations. The new synthesizer is based on the state-of-the-art DDS chip by Analog Devices (AD9915), which will be externally controlled by an field-Programmable gate array (FPGA). This DDS chip has a lower phase noise than the AD9954 and interfaced with the FPGA, this versatile frequency synthesizer will provide high flexibility for arbitrarily phase ramps.

Expected improvements with the versatile digital frequency synthesizer

The AD9915 DDS chip has a 32-bit phase accumulator and a 16-bit phase offset word for phase modulation. The main reason this chip was opted for is the ability to send the phase offset word to the DDS in in a time (10ns) much shorter than the response time (1us) of the transport system. The latter is essentially limited by the finite bandwidth of the AOM used to control the phase of the lattice beams. The AD9915 has a parallel port that can be used to modulate the frequency, phase or amplitude. This is an advantage over the AD9954 since we could store only 1000 phase points between four sequences on the on-board static random-access memory (SRAM) of the AD9954. These 1000 phase points were transferred to the SRAM over a serial bus from a micro-controller. The capability to

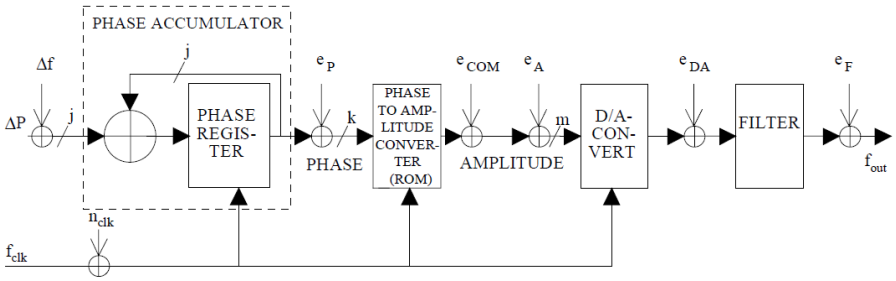

Figure 2.11: Block diagram showing the noise contributions to the DDS. Figure taken from [37]

stream phase points in real-time overcomes the limitation of 1000 data points. Figure 2.10 shows the discrete nature of a transport ramp over 100 lattice sites with the previous DDS (AD9954) and the expected improvement with the versatile frequency synthesizer.

For an estimate of the number of phase points required to achieve a long distance interferometer, we have to take into the account the bandwidth of the system. The transport ramp for the atoms has to be optimized such that states $|\uparrow\rangle$ and $|\downarrow\rangle$ undergo minimal excitation while being transported. Taking into consideration the fact that the two spin states experience a wobbling potential while being transported, the optimal time required to shift a state by one lattice site is $20\,\mu s$ [48]. Hence transporting the atom over n lattice sites requires $20n\,\mu s$, under the assumption that time required scales linearly with distance. In order to achieve a smooth transport ramp, the time interval between the phase points must be less than the bandwidth of the system. Hence for M phase points, the number of lattices the atom can be shifted by is given by the condition:

$$\frac{n \cdot 20}{M} \leqslant 1$$

Therefore, with the 1000 data points that can be stored on the AD9954 DDS chip, the maximum distance attainable for an interferometric sequence is 50 lattice sites. To achieve a long distance interferometer with splitting of the order of 1 mm, the atom needs to be transported over more than 2000 lattice sites. Hence the minimum number of phase points required is around 40,000. The FPGA that will send data in parallel to the AD9915 can store over a million data points, a major improvement over the AD9954 chip.

Furthermore, the chip uses a 2.5 GHz reference clock allowing for a higher update rate of 6.4 ns (the internal clock works at 1/16th the reference clock) [49]. The AD9915 is capable of achieving a frequency resolution of 136 pHz and a phase resolution of $9.59{\cdot}10^{-5}$ radians [49] .

Expected improvement in the phase noise

To predict the improvement in phase noise over the AD9954 DDS, we use a model for phase noise in digital synthesizer. A direct digital synthesizer has six sources of noise and spurious frequencies [37] that are shown in figure 2.11. The noise contributions as the signal moves through the different functional blocks first begins before the look-up table

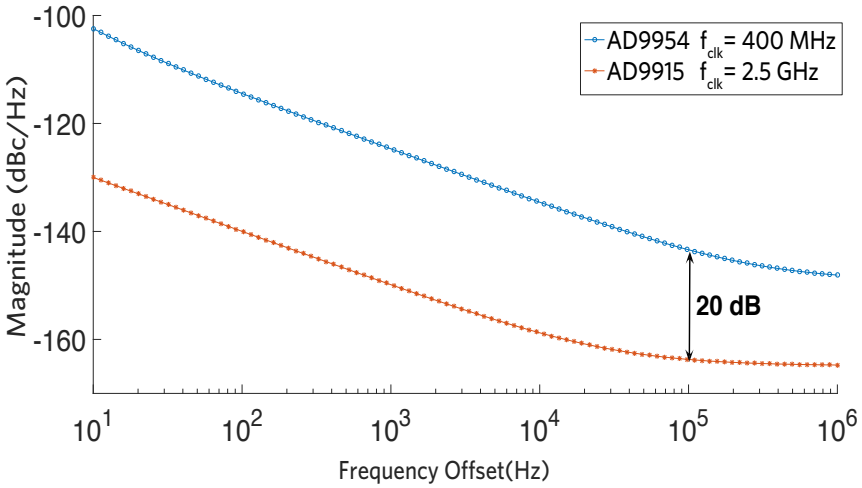

Figure 2.12: Extrapolated single sideband spectrum for the two DDS chips: AD9915 and AD9954. There is a suppression of noise by around 20 dB at an offset of 100 KHz. The reference clocks for the two are different.

where truncation of the output from the phase accumulator gives an error e_P. The next source of error e_{COM} comes from the fact that a compression algorithm is used in the look-up table in order to minimize space [37]. The symmetric property of the sine wave is used to reduce the number of data points the look-up table needs for converting phase to amplitude. e_A is contributed from the imprecision of the phase to amplitude conversion of the look-up table. e_{DA} is the noise contribution from the digital to analog converter while e_F is the contribution from the filter. The reference clock used by the DDS also introduces noise n_{clk} to the output. In most cases, it is the noise of the reference clock that limits the noise of the output signal.

The phase noise of direct digital synthesizers has been empirically modeled in [50, 51]. It is given by

$$S_{\mathrm{DDS}}(F) = (K_{\mathrm{DDS}})^2\left(\frac{10^{k_2}}{F^2} + \frac{10^{k_1}}{F} + 10^{k_4}\right) + 10^{k_3} + S_q \ , \tag{2.21}$$

where S_{DDS} is the power spectral density of the DDS phase noise. $K_{DDS} = f_{out}/f_{clk}$, the ratio of the synthesized frequency to the clock frequency. k_2 and k_1 are the coefficients for the contribution from $1/F^2$ and $1/F$ (flicker-noise) noise respectively. k_4 is the coefficient for the noise contribution from the various noise sources discussed above and k_3 is the coefficient for noise from the resistive load. S_q is the quantization noise of the digital to analog converter.

I fitted the model to the phase noise spectra provided by data sheets for both AD9915 and AD9954 DDS chips. This allowed me to obtain the values of the coefficients. Since the electronic reference is set at a frequency of 80 MHz in the experiment, I extrapolated the phase noise of the two DDS chips for this frequency, as shown in figure 2.12.

Figure 2.12 shows the single sideband noise spectrum for the two chips at a carrier

frequency of 80 MHz. Along th y-axis is the power of the signal at an offset frequency measured in a 1 Hz window divided by the power carried by the carrier. This single sideband spectrum is directly proportional to the power spectral density S_ϕ. As we have seen in section 2.5, the heating rate is directly proportional to S_ϕ. At the offset of around 100 kHz (close to the trap frequency), the phase noise is roughly 20 dBc lower for the AD9915. This corresponds to a suppression of S_ϕ by two orders of magnitude and hence a reduction of the heating rate by two orders of magnitude.

3

A versatile digital frequency synthesizer

This chapter reports on the development of the new versatile frequency synthesizer, whose advantages with respect to the previous setup have been discussed in the receding chapter. Figure 3.1 shows how the FPGA based frequency synthesizer will be implemented in the existing optical phase locked loop (see section 2.4). Two of the three DDS chips will serve as the electronic references for the two circularly polarized beams while the third DDS is used to directly drive the AOM for the counter-propagating beam(see fig. 2.5 in section 2.3). Precise control of the phase of the counter-propagating beam allows us to perform common mode accelerations or transport as required in the experimental realization of electric quantum walks [52].

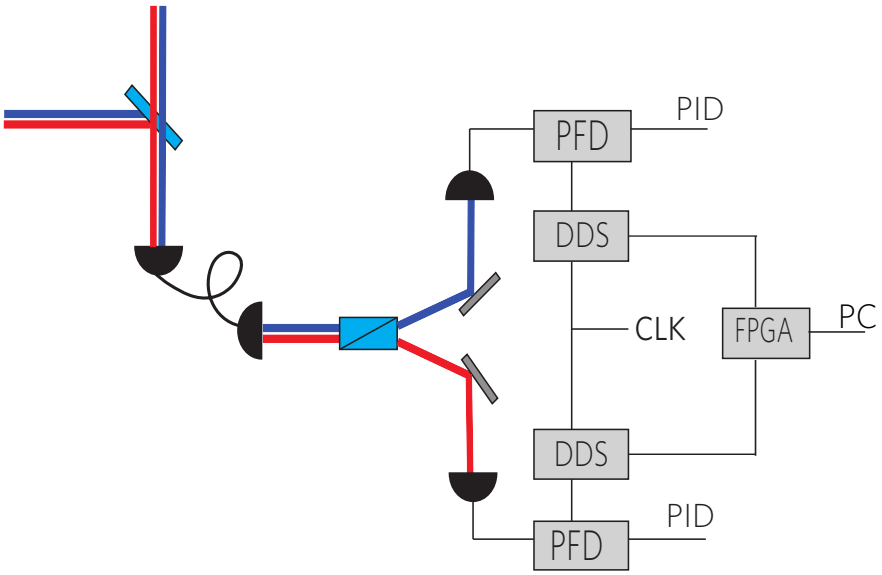

Figure 3.1: Schematic of the optical phase lock loop with the proposed control of DDS boards using an FPGA

The next section briefly introduces FPGAs, discussing its architecture and advantages. The rest of the chapter gives a description of the versatile digital frequency synthesizer.

3.1 Field programmable gate arrays

Field programmable gate arrays are prefabricated silicon devices that can be programmed to function as an arbitrary digital circuit or system. In contrast to application specific integrated chips (ASICs) that fulfill specified predetermined functions, FPGAs provide a generalized hardware platform that can be programmed (and reprogrammed nearly an unlimited number of times) by modifying the firmware specific to the design [53]. In addition to the re-programmability, what makes FPGAs powerful tools is their ability to perform parallel functions simultaneously and the ability to manage several high speed digital clocks. Because of this flexibility, FPGAs are widely used in high-energy and nuclear physics experimental setups [53]. Because the AD9915 chip has a parallel data port that can be used to modulate the phase of the output, FPGAs are well suited to externally control the AD9915 DDS chip.

FPGA architechture

The primary building blocks of an FPGA are logic elements (logic cells). These logic cells generally consist of a 4-input look-up table (LUT) for combinational logic and a flip-flop for sequential logic. These logic blocks are organized as arrays on the FPGA chip. In case of an operation that requires more than four inputs, the flip-flop can be bypassed and multiple LUTs can be cascaded together to perform the function. The LUT is a 16bit random access memory (RAM) and its contents are loaded when the FPGA is programmed. In addition to the logic elements, FPGAs also have RAM blocks which are used to buffer both input and output data which can be streamed serially or in parallel. FPGAs also have function specific hardware resources to save logic resources, reduce power consumption and to simplify routing of commonly used components such as a multiplier. A schematic of the FPGA structure is shown in figure 3.2.

An advantage FPGAs have over microprocessors is their parallel computational power. A basic microprocessor architecture contain one processing unit, known as the arithmetic logic unit. A processing unit performs one computation per clock cycle, hence performing N computations in N clock cycles. FPGAs, on the other hand, have flat designs. They have multiple processing units that perform an operation every clock cycle. This way N computations can be done with one clock cycle on an FPGA by using N processing units. The trade-off here is the space used. As the number of processing units increases, the amount logic cells required increases too.

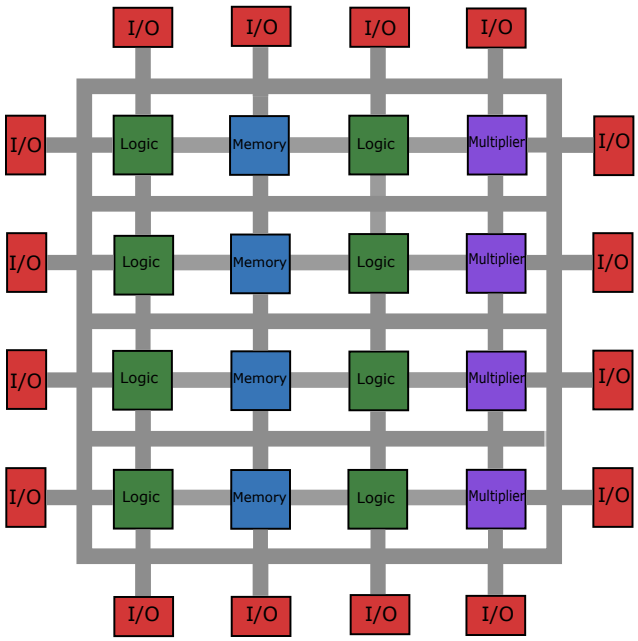

Figure 3.2: A simple schematic showing the basic architecture in an FPGA. All the different components are interconnected by programmable routing fabric

Cyclone IV FPGA for controlling the digital synthesizer chip

An FPGA development board, DE2-115 [54], containing a Cyclone IV FPGA chip[1] is used to control the AD9915 DDS chip. The Cyclone IV FPGA device has 114,480 logic elements, 3.8 Mbits of embedded memory and 266 embedded multipliers [55]. In addition to this, it has 4 phase locked loops to generate high frequency clocks from base clocks. The FPGA chip has 528 user I/O pins, some of which are already connected to the on-board peripherals. The DE2-115 development board is used because it has large amounts of peripheral memory to store data points for the DDS, and an Ethernet port which will be used for high speed data transfer from the computer.

In comparison to the new versatile digital frequency synthesizer, the previous DDS board (AD9954) is controlled by a micro-controller. While micro-controllers are suitable for serial data transmission, they are not feasible for parallel processing. In our design, we want to transmit data in parallel to the DDS chip to modulate the phase of the output signal. Furthermore, the FPGA performs other tasks in parallel such as generating triggers for different sequences. The FPGA also manages multiple high frequency clocks that are generated on the chip with fixed phase differences. These clocks can simultaneously run different digital processing blocks on the chip. This flexibility coupled with its parallelism gives FPGAs a definitive advantage over micro-controllers for our specific project.

[1] Cyclone EP4CE115

Since the DE2-115 development board is used in the project, henceforth, the term FPGA always refers to the evaluation board, unless stated otherwise. Likewise, the AD9915 DDS chip too is available on a development board[2] and when I mention DDS I allude hereafter to the development board unless specifically stated otherwise. The advantage of using the development boards is that they come with additional hardware features such as external memories and Ethernet sockets in the case of the FPGA or filters and SMA connectors in the case of the DDS.

The FPGA-based synthesizer is locked to a 2.5 GHz reference clock which is generated from a digital frequency synthesizer [3]. All other clocks running in the versatile digital frequency synthesizer are managed by the FPGA chip and will be discussed in subsection 3.3.2.

3.2 Overview of data flow

The FPGA will send data to the DDS in real-time, allowing us to modulate the phase with nanosecond precision, limited by the sampling time of the chip. In order to perform transport sequences, we want the DDS to perform a set of different phase ramps in response to a transistor-transitor logic (TTL) trigger which is executed in an experimental sequence.

The data transmission process to the versatile digital frequency synthesizer can be grouped into two main categories: programming mode, where data is transferred to the FPGA, and streaming mode, where the data is streamed to the DDS. While the programming mode is not directly

3.2.1 Programming mode

The programming mode encompasses data transfer from the PC to the FPGA, reallocation of data within the FPGA board and programming the DDS registers for frequency, amplitude and phase settings. All these functions are performed before the execution of the experimental sequence and do not require real-time programming. The programming mode also handles large streams of data for phase ramps which are transferred from the PC to the FPGA board.

The data flow begins at the PC where the experimental physicist decides which array of phase points are to be sent to the FPGA over Ethernet, via a TCP connection established by Matlab®. This incoming data is stored on an external synchronous dynamic random access memory (SDRAM) connected to the FPGA chip. The data consists of multiple transport sequences, each of which can contain over a 100,000 16-bit phase words that will later be sent to the DDS boards in real-time.

The 128 MB of memory offered on the SDRAM is sufficient to store multiple sequences of data in order to prevent programming mode for later sequences. This is done to quickly

[2] Eval-AD9915
[3] AD4351 from Analog Devices

switch between sequences that we might want to perform in the experiment, avoiding time-consuming transfer operations from the PC every time a new sequence is needed.

Once the transfer of all data from the PC is complete, we can choose sequences that are to be carried out in the specific experiment. These are transferred to the 2 MB of internal SRAM on the board that can operate at higher frequencies. It has a 16-bit data bus, which is the number of bits that constitute a phase word.

As mentioned before, the transfer from PC to SDRAM and from the SDRAM to the SRAM are not time critical which is why they can be handled by a soft-core microprocessor that runs on the FPGA chip. The soft-core microprocessor runs a real-time operating system (MicroC) that is programmable in C, which makes it easier to program the Ethernet management on the FPGA. Being able to run a microprocessor on the FPGA chip highlights the flexibility of these devices, which can be programmed to perform any function the user desires.

Finally, certain fixed parameters of the DDS, e.g. frequency and amplitude are set by programming the DDS registers in parallel. The data for the different registers are sent over Ethernet connection and managed by the soft-core processor and a general purpose input output (GPIO) controller that I programmed in the hardware description language. This gives us the ability to access and configure the registers of the DDS directly via Matlab®, which is used to control the experiment. Once the DDS register values are set, the data for phase modulation is streamed from the SRAM as discussed in the next section.

3.2.2 Streaming mode

The streaming mode is concerned with the time critical streaming of data to the DDS for phase modulation. This mode is time critical because the phase modulation happens in real-time for transporting the atoms in optical lattices. A 16-bit data word is transmitted on each clock transition that runs at 156 MHz delivered by one of the DDS boards as shown in figure 3.3. Sharing a clock between the DDS and the FPGA is necessary to ensure a synchronous data transmission. Using unsynchronized clocks for data transmission can lead to metastability issues for the DDS (see section 3.3.2).

The data streaming begins when a PC generated TTL signal is received by the FPGA chip on one of 4 port for receiving external TTL signals. I programmed the FPGA to react on different combinations of the TTL signals that will decide which sequence to stream and which DDS board to address. Since the TTL signal is generated by the PC, we expect a delay in time before it reaches the FPGA to start phase modulation. This delay can in principle be measured and compensated via feed-forward.

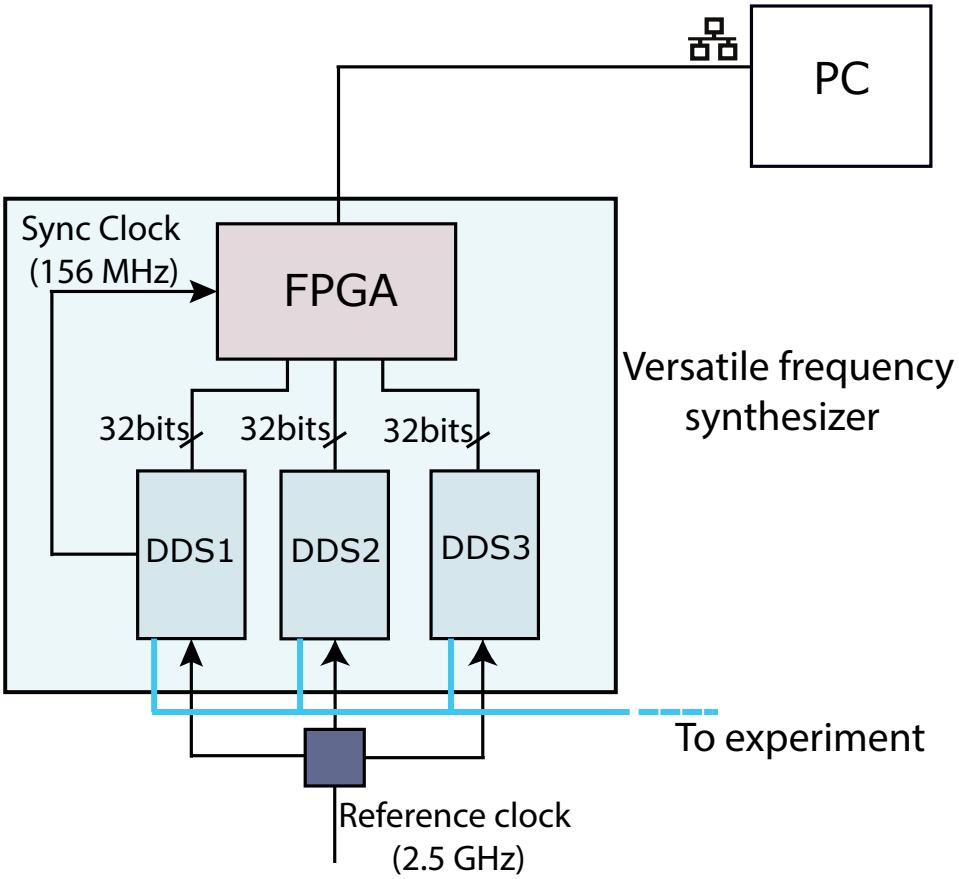

Figure 3.3: Block diagram of the versatile digital frequency synthesizer.

3.3 Handling data

In this section I will briefly report the work done in order to handle data on the FPGA. This is followed by a description on the different clocks domains in use on the FPGA chip. Finally, I will discuss the debugging tools used to program a field-programmable gate array.

3.3.1 Wiring up the FPGA

A block diagram of the FPGA board used in the project is shown in figure 3.4. The FPGA chip is interfaced with many different additional peripheral components such as external memories, high speed mezannine card (HSMC), VGA ports, USB ports and so on. The peripherals used in this project are the Ethernet socket (RJ45), external memories (both SRAM and SDRAM), USB blaster, LCD module, 50 MHz oscillator, clock ports, HSMC and the general purpose input-output ports.

As discussed in section 3.1, one of the main advantages of using field-programmable gate arrays is their ability to process data in parallel. This is required to execute, for example, a phase ramp on all three DDS boards simultaneously and synchronous to a single input

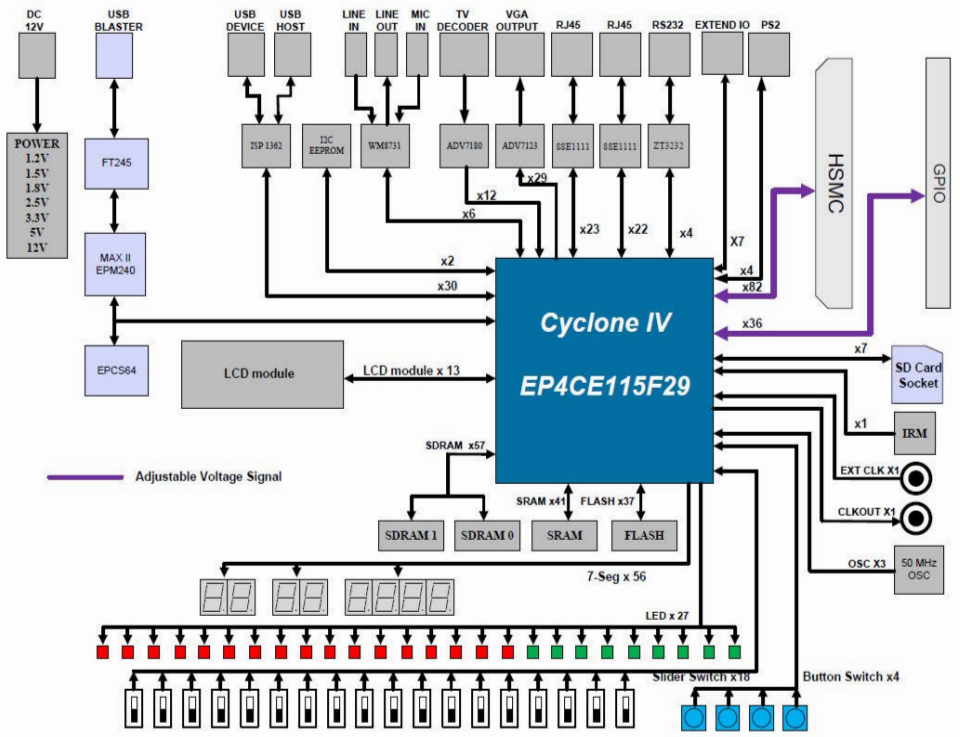

Figure 3.4: Block diagram of the FPGA board used, the DE2-115. Figure taken from [54].

trigger. Such parallelism is achieved by hard-wiring every function of the program onto the gates of the device. These gates, which generally work as look-up tables, perform their specific function independently of each other on every clock edge.

Due to this parallel working principle of FPGAs, they can not be programmed with the same principle of high level software programming languages such as C. Programming an FPGA is more demanding since it involves hardware description language (HDL). The HDL used in this project is Verilog. While code written in software programming languages is a set of instruction for the CPU to perform a series of basic operations, a code written in HDL is directly transposed into hardware. Unlike C, HDL code is not written for sequential operation. This means that all functions in a program are carried out by different logic units of the FPGA, enabling them to work in parallel. Another important difference between the two is that in HDL we can impose timing limitations for interfaces between blocks, which software programming languages cannot. Fulfilling timing requirements is very crucial for electronic circuits in order for them to function properly. Lastly, given that every line of code written in HDL is transposed to a direct hardware implementation, it is essential to iteratively optimize the code in order to not use up all the logic resources. Optimizing the code to minimize logic resource usage is extremely crucial when programming FPGAs.

Since some interfaces for peripheral devices are very complex to program, the FPGA chip manufacturer, Altera, provides pre-programmed modules known as intellectual property (IP). Figure 3.5 is a block diagram of the most important modules used on the FPGA

chip. The Ethernet interface and SDRAM controller are IPs provided by Altera, which do not need any modification except providing them with the correct clock signals to the modules. The SRAM controller and the general purpose input-output (GPIO) controller were programmed in Verilog. The GPIO controller manages both the GPIO peripheral and the HSMC shown in figure 3.4. The high speed mezzanine card is a dense collection of input-output (I/O) pins that be distributed out using a breakout board. This is used to transmit data to the DDS boards. Figure 3.5 also includes a block called NIOS II. This is a propriety 32-bit soft-core processor that is synthesized onto the hardware to manage some of the data transfer, as discussed. NIOS II is programmed in C to perform certain tasks, such as implementing a TCP/IP protocol for data transfer over Ethernet and storing instruction sets for data handling as well as instructions that execute commands sent from Matlab®. All the software files related to the sof-core processor are stored on the SDRAM.

The soft-core processor reads the set of commands sent from Matlab® to decide whether data should be stored on the SDRAM or whether the DDS parameters have to be set. If the incoming data is sequences for the ramp, the processor routes this data to a given memory location on the SDRAM. Otherwise, the data is sent to the GPIO controller. This interface between a C programmed processor and a Verilog programmed controller is managed by the internal bus fabric provided by the FPGA designing software, Quartus. Depending on which DDS board and register the data is directed to, the GPIO controller sends the required update pulse and address access bits to the DDS followed by the data sent from Matlab®.

For data that corresponds to sequences, the array of phase words is routed by the soft-core processor to the SDRAM. Since the SDRAM already stores some of the software files used by the processor it is important that a separate location on the SDRAM is alloted for the sequences. On the next set of commands from Matlab®, the user chooses which ramps will be implemented in the experiment. The soft-core processor stores the starting address of every sequence in an array and once it gets the sequence numbers, it copies these specific sequences to the asynchronous SRAM[4] on the board. An asynchronous memory is not dependent on the clock frequency for data transfer. The data transfer is controlled by address transition. This is particularly suited for us since the processor runs at a different clock speed than the speed with which we want to stream out data from the SRAM and hence both the processor and the GPIO controller can independently use the SRAM. The 2 MB of storage space on the SRAM is entirely used for storing the sequences to be executed in the following experimental sequence.

After all the sequences have been copied, the GPIO controller waits for a TTL signal from the PC. This 3.3 V signal is delivered to an input pin which then triggers the streaming of data from the SRAM. The GPIO controller reads out data points from the SRAM at the DDS internal frequency, 156 MHz.

[4] ISSI-IS61WV102416BLL

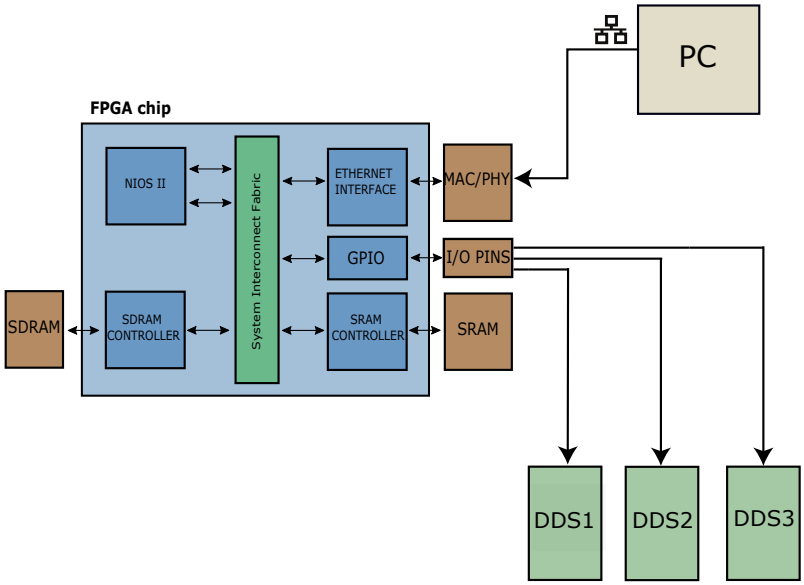

Figure 3.5: Schematic of the different modules used on the FPGA chip to communicate with the external peripherals. The double-sided arrows denote data transfer and the additional arrow for NIOS is the instruction set.

3.3.2 Clocking the FPGA

Identifying the number of clocks needed in a design and how to route them is one of the most crucial tasks in building a project. The ability of field-programmable gate arrays to manage several digital clocks at different frequencies let us split up the different tasks to be performed based on whether they are time critical or not (see sec. 3.2). On the chip, each region working at a given clock frequency is known as a clock domain. While programming the FPGA one needs to make sure the timing requirements between different clocking domains are met. The DE2-115 board has a 50MHz oscillator on board(see figure 3.4). Using this source as a base clock, clocks of higher frequencies are generated through a phase lock loop (PLL). Table 3.1 notes the different clocks in the project and the components that use them.

Clock Name	**Frequency**(MHz)	**Usage**
Clock-50	50	base clock for PLL
Sys-clk	100	NIOS II
IO-clk	10	LEDs, switches
sdram-clk	100	SDRAM
enet-rx-clk	125	Ethernet
SMA-clkin	156	Data transfer to DDS

Table 3.1: Different clocks used in the project with their corresponding frequencies and usage

Clock-50: The 50 MHz clock used as a base clock for the PLLs on board is a stable

source to run all operations related to data transfer between the computer and the FPGA. These are all the processes that are not critical in time.

Sys-clk: The Sys-clk is the system clock that is used to clock the soft-core processor. The Sys-clk is derived from the 50 MHz base clock. Data transfer to and from the Ethernet module is also clocked using the Sys-clk.

IO-clk: The IO-clk is used to clock peripherals that do not need to operate at high frequencies. Some of these peripherals are LEDs on the board, switches and the LCD display. Communication between the processor, running at 100 MHz, and these peripherals running at one-tenth the speed is managed using a clock crossing bridge. A clock crossing bridge adds a first-in, first-out (FIFO) buffer between the two components running at different frequencies. The reason why a slower clock domain is used for the peripherals when they can in principle work at higher frequencies is in order to ease the optimization of where the different registers should be suitably placed. Fitting the registers is automatically done by the FPGA design software Quartus once the design is compiled. The registers are fit in order to achieve the timing requirements set by the experiment, which means registers of a given clock domain are generally grouped together. If high speed clock domains are small and not spread across different regions in the FPGA chip, it becomes easier to optimize the placing of registers in order to reach high frequencies of operation.

sdram-clk: The sdram-clk, as the name suggests, is used to communicate with the SDRAM. It also runs at 100 MHz but is phase shifted with respect to the Sys-clk. This is done to ensure that the data on the SDRAM pins are stable when the positive clock edge arrives at the clock pin of the SDRAM. The data is transferred to the SDRAM pins on the positive edge of the Sys-clk. The data reaches the pins 3 ns before the positive edge of the sdram-clk arrives. The phase shift between the two clocks is adjusted using the PLL, as both the Sys-clk and the sdram-clk are sourced from the 50 MHz base clock.

enet-rx-clk: The enet-rx-clk is a base clock used between the Ethernet interface and the physical layer chip (PHY). Derived from the enet-rx-clk is a clock used for data transfer from the media access control (MAC) to the PHY device and another clock used for data transfer from the PHY device to the MAC. There is a phase difference of 90° between these two clocks in order to handle data transfer on the correct clock edge.

SMA-clkin: Finally, we have the time critical SMA-clkin clock used for communication between the FPGA and the DDS. The DDS chip has an internal clock which runs at one sixteenth the frequency of the reference clock that is fed to it. In our case, the reference clock has a frequency of 2.5 GHz, the maximum possible for the AD9915. We choose to use the maximum possible reference clock because higher sampling clocks for the DDS lead to lower phase noise for the DDS output (refer to equation 2.21 in section 2.6). The internal clock runs at 156.25 MHz. One of the DDS boards provides this clock to the FPGA (it is called Sync clk in figure 3.3). This board will henceforth be called the master board. The 2.5 GHz reference clock provided to the DDS from a synthesizer is phase locked to a rubidium-disciplined crystal oscillator, operating at 10 MHz, that is used as a frequency reference in the laboratory. As a result, the SMA-clkin is also locked to the 10 MHz reference. This is very important because data transfer to the DDS is time critical. And since this data consequently leads to the transport of atoms, the clock it is

streamed at has to be locked to a stable reference. All data that is sent to any one of the DDS boards is transmitted on the positive edge of the SMA-clkin. It is important to use this clock for data transfer because we want to have precise control over the phase modulation of the DDS. Using a clock that is not synchronous with the internal clock of the DDS can lead to metastability issues. The DDS latches onto new incoming data on the positive edge of the internal clock. Metastability here means that if data from the FPGA is being sent on the positive edge of a different clock then there is a possibility that the data does not reach the DDS chip in time for it to be latched on to. This would cause unwanted delays in our transport sequence and unexpected phase modulation. Another reason the SMA-clkin is important is because it is used to synchronize the three DDS boards.

3.3.3 Synchronizing the DDS chips

Since the internal clock of the DDS runs at 1/16 of the reference clock, it has sixteen possible positive edges of the reference clock that it can align its own positive edge to. When the DDS boards are turned on, the internal clock for each of the boards can start in any one of the sixteen states. For our application, we want all the internal clocks to be edge aligned to each other. The synchronization protocol [56] requires that each of the DDS boards receive a clock from a *master board* in order to synchronize with each other. In the scheme provided, a synchronization clock is taken from one of the boards and using a clock buffer redistributed to the three boards(including the master board). This synchronization clock has a frequency of roughly 6.5 MHz. In our project, instead of using the synchronization clock, we use the internal clock of the master DDS that we already use for data transfer. The internal clock is divided down to 19.5 MHz on the FPGA and sent to the DDS boards, as shown in figure 3.6. The idea here is to edge align the synchronization clock sent from the FPGA and the internal clock of the DDS board. I had to take into account different design considerations to achieve proper synchronization: The reference clocks being fed to the DDS boards need to be synchronous with each other (the clock edges must be aligned with each other) and the synchronization clocks being sent to the DDS chips from the FPGA also needs to be synchronous with each other. This can be achieved by using the same length of cables used to connect to the DDS boards.

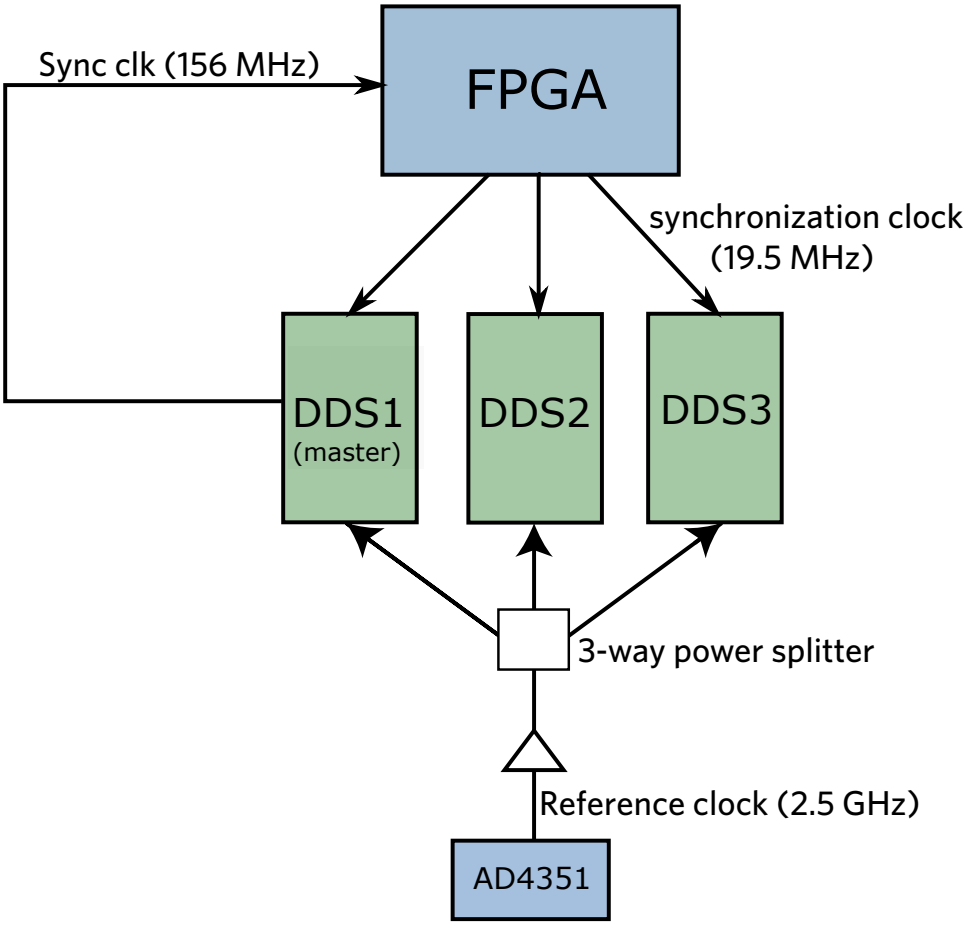

Figure 3.6: Block diagram of the different clocks and components used for synchronizing the DDS chips.

3.3.4 Debugging tools for FPGA programming

The Verilog code for the FPGA was written using the Quartus framework. This is propriety software provided by Altera for their FPGAs. Quartus analyses the code and synthesizes it to hardware. Synthesis here means converting the code written in Verilog to a combination of logic gates. Before doing so, it fits the design for the specific FPGA chip and runs a timing analysis of the design. The general architecture of the project in Quartus requires a main file with the declaration of all the I/O ports that will be used in the project. This file is known as the top level file. Other modules are then instantiated in this top level file with the respective assignments for the I/O ports. These I/O ports are assigned to the different pins of the FPGA chip in the Quartus settings file. Here one can define the voltage levels of the signals to be transmitted from a given pin.

The timing constraints for the design are defined using a synopsys design contraints (SDC) table. Once we write the SDC table for the specific timing requirements, the software attempts to place the registers in order to meet the specific requirements. The timing analyzer is executed to check whether the design meets and timing requirements

and hence in an iterative way, by modifying the SDC table and using the timing analyzer, the design proceeds further with the optimization by modifying the SDC table and repeating the time analysis. Another tool that I used for debugging is the SignalTap Logic Analyzer. SignalTap is used to probe signals on the FPGA in real-time. It works as an on-board oscilloscope where one can set the trigger conditions and capture the data being sent through different registers on the FPGA. The data is sent through a JTAG connection to the computer where it is plotted like if I recorded the physical signal with a external probe on an oscilloscope. The registers that are probed have to be defined before compiling since the fitter has to create a physical route for data from the registers to the JTAG adapter. Furthermore, a sampling clock has to be defined for SignalTap in order for it to capture data on the positive(or negative) edge of this clock.

4

Phase noise of the versatile digital frequency synthesizer

The importance of minimizing the phase noise of the optical lattice beams for state dependent transport has been discussed in chapter 2. Furthermore, in section 2.5, I have shown that the atom's lifetime has been hitherto limited by the phase noise of the AD9954 DDS chip. As displayed in figure 2.12, which shows the phase noise of the AD9954 and AD9915 DDS chips extrapolated from their data sheets, we expect a reduction of phase noise by $\sim 20\,\mathrm{dB}$ at the trapping frequency of the optical lattice with the new AD9915 chip. In the following chapter I describe how I measured the phase noise of the frequency synthesizer and I compared it to the values reported in the data sheet.

4.1 Phase noise

Phase noise results from small random fluctuations in the phase of an electronic signal. For a direct digital synthesizer, the phase noise at a small frequency offset from the carrier is highly dependent on the phase noise of the reference clock [57]. This output of the DDS can be modeled as:

$$V(t) = V_0 \sin(2\pi\nu_0 t + \phi(t)),$$

where V_0 is the amplitude, ν_0 the frequency and $\phi(t)$ is the random phase fluctuation denoting phase noise [58]. Such phase fluctuations are better understood in the frequency domain, where we define power spectral density $\mathrm{S}_x(f)$, which tells us how the variance is distributed over the frequency components. It is also defined as the power contained in a one hertz band at an offset frequency f and is measured in units of V^2/Hz. S_x is related to the one-sided spectral density of phase noise, $\mathrm{S}_\phi(f)$, which has units of $\mathrm{rad}^2/\mathrm{Hz}$.

While it is natural to think of phase noise in units of radians, the IEEE defines phase noise (L_ϕ) in units of dBc/Hz [59]. Under the assumption that $\phi(t)$ is much smaller than 1 radian, $\mathrm{L}_\phi(f)$ can be related to $\mathrm{S}_\phi(f)$ as:

$$\mathrm{L}_\phi(f) = 10\log[\frac{1}{2}\mathrm{S}_\phi(f)]$$

If the small angle condition is not met, Bessel functions corresponding to higher-order terms of a certain Jacobi–Anger expansion must be used to relate the two terms [59]. The small angle condition was met by our particular setup, and hence I could rely on $L_\phi(f)$ in order to measure the phase noise and compare it with the data sheet specifications.

4.2 Phase noise characterization

The experimental setup used to measure the residual phase noise of a DDS board is shown in figure 4.1. In order to understand the concept behind such a setup, let us assume the two DDS boards DDS1 and DDS2 generate a sinusoidal and co-sinusoidal wave with frequencies ω_1 and ω_2 respectively, given by:

$$\begin{aligned} & V_1(t) = A_1 \sin(\omega_1 t + \phi_1(t)) \\ \text{and} \quad & V_2(t) = A_2 \cos(\omega_2 t + \phi_2(t)), \end{aligned}$$

where phase instability is contained in the constants $\phi_1(t)$ and $\phi_2(t)$ [60]. Mathematically, the mixer multiplies the two input signals and its output is given by:

$$\begin{aligned} V_{out}(t) &= \alpha \cdot V_1(t) \cdot V_2(t) \\ &= \frac{1}{2}\alpha A_1 A_2 \cdot \sin((\omega_1 - \omega_2)t + \phi_1(t) - \phi_2(t)) + \frac{1}{2}\alpha A_1 A_2 \cdot \sin((\omega_1 + \omega_2)t + \phi_1(t) + \phi_2(t)), \end{aligned}$$

where α is the mixer conversion constant. If the frequencies ω_1 and ω_2 are set equal to each other (ω_1=ω_2=ω), the output is given by:

$$V_{out}(t) = \frac{1}{2}\alpha A_1 A_2 \cdot \sin(\phi_1(t) - \phi_2(t)) + \frac{1}{2}\alpha A_1 A_2 \cdot \sin(2\omega t + \phi_1(t) + \phi_2(t)). \tag{4.1}$$

Using a low-pass filter, we can suppress the sum frequency, giving:

$$V_{LPF}(t) \approx \frac{1}{2}\alpha A_1 A_2 \cdot \sin(\phi_1(t) - \phi_2(t)). \tag{4.2}$$

The phase of the DDS signals can be tuned such that $\phi_1(t) \approx \phi_2(t)$. Then using the small angle approximation we have:

$$V_{LPF}(t) \approx \frac{1}{2}\alpha A_1 A_2 \cdot (\phi_1(t) - \phi_2(t)) \tag{4.3}$$

$$= \frac{1}{2}\alpha A_1 A_2 \cdot (\Delta\phi(t)), \tag{4.4}$$

where $\Delta\phi(t)$ is the difference between the phase fluctuations. Hence the signal at the output of the low-pass filter is proportional to the difference in the phase noise contribution of the two DDS boards.

In order to calculate the phase noise from our data, we need to find the value of $\alpha A_1 A_2$,

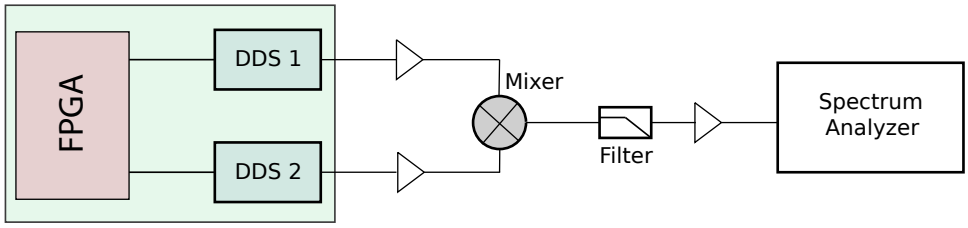

Figure 4.1: Setup for residual phase noise measurement. Two signals with equal amplitude and frequency but 90° phase difference are mixed using a mixer which generates a voltage proportional to the phase fluctuations between the two signals. The high frequency product from the mixer is filtered out using a low pass filter.

the proportionality constant in equation 4.4. Since $\Delta\phi(t)$ is a random process, we can only deal with statistical quantities, for example,the mean squared voltage [60]:

$$\overline{V_{LPF}^2(t)} = \left[\frac{\alpha A_1 A_2}{2}\right]^2 \cdot \overline{(\Delta\phi(t))^2} \tag{4.5}$$

$$\tag{4.6}$$

Taking a square-root on both sides, we define a mixer conversion factor K_ϕ:

$$K_\phi = \frac{\sqrt{\overline{V_{LPF}^2(t)}}}{\sqrt{\overline{(\Delta\phi(t))^2}}} \quad \text{V/rad} \tag{4.7}$$

Although the constant K_ϕ here is written for a random variable $\Delta\phi$, it is valid for deterministic signals and holds for instantaneous as well as time averaged values[60]. The mixer constant then equals:

$$K_\phi = \frac{\alpha A_1 A_2}{2}.$$

In order to calculate K_ϕ, I use the setup as shown in figure 4.1 except for using an oscilloscope instead of the spectrum analyzer. From equation 4.4 we know that for $\phi_1(t) \approx \phi_2(t)$, the output is linearly proportional with mixer conversion factor K_ϕ. By programming the phase offset word of the DDS boards, we meet this condition. By digitally changing the phase of one of the DDS boards, we note the increase in voltage. The phase step of the DDS is exactly known and is given by $\frac{2\pi}{2^{16}}$ radians for an increment of one bit in the phase offset word. By noting the voltage change corresponding to a phase change of the DDS, the mixer conversion factor K_ϕ can be determined. The voltage change of the mixer output is plotted against the phase increment of the DDS in figure 4.2. The slope of the curve gives K_ϕ which is 0.91 V/Hz for the mixer used.

With K_ϕ extracted, we need to measure the power spectral density of the mixer output. Two DDS boards of the versatile digital frequency synthesizer were programmed to generate a fixed frequency of 123 MHz. The amplitude of both the signals was fixed at

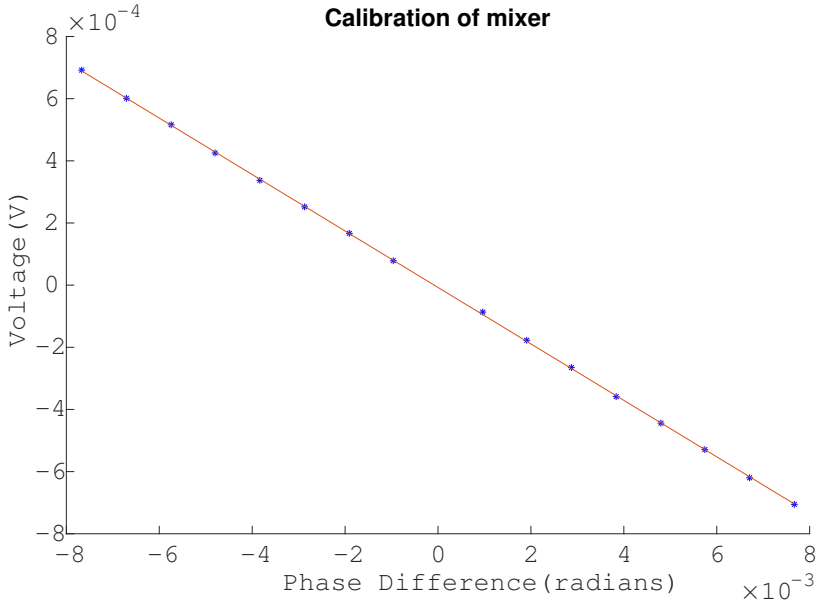

Figure 4.2: Calibration of the mixer constant. The phase difference of one of the DDS boards is incremented and the corresponding output voltage of the mixer is noted. The slope gives the mixer constant K_ϕ which is 0.91 V/rad.

-0.4 dBm, the maximum attainable from the synthesizers. This signal was amplified to 7 dBm to match the specifications of the mixer[1]. A low pass filter with a cut-off frequency of 11 MHz was used to suppress the sum frequency. The output of the filter was amplified using a low-noise pre-amplifier before being sent to the spectrum analyzer.

The pre-amplifier is used to amplify the signal above the noise floor of the spectrum analyzer. The caveat in this measurement is that the noise at the output of the pre-amplifier will also contribute to the noise measurement. In order to characterize this, a measurement is taken where the input is terminated by a 50Ω resistance and the gain of the pre-amplifier is increased until a noticeable noise signal is detected. This means that the output noise of the pre-amplifier is below the noise floor with the current gain settings. Using this method, the gain was set to 50,000. Figure 4.3 shows the power spectral density of the mixer output measured for the setup described above.

The measurement described above includes the noise contributions from other components in the setup, such as the amplifiers. In order to deduct their contribution, a reference measurement has to be performed. The setup for the measurement is shown in figure 4.4. Here both input signals to the mixer are from the same DDS board. This means ideally the output of the low-pass filter should be zero since there is no differential phase noise between the two inputs of the mixer. But in reality, since active components such as the amplifiers contribute phase noise, the spectrum analyzer measures the noise of such components. The noise is used as a reference and it is subtracted from the phase noise measurement between the two DDS boards. The power spectral density of the reference

[1] Mini-circuits ZFM-3+

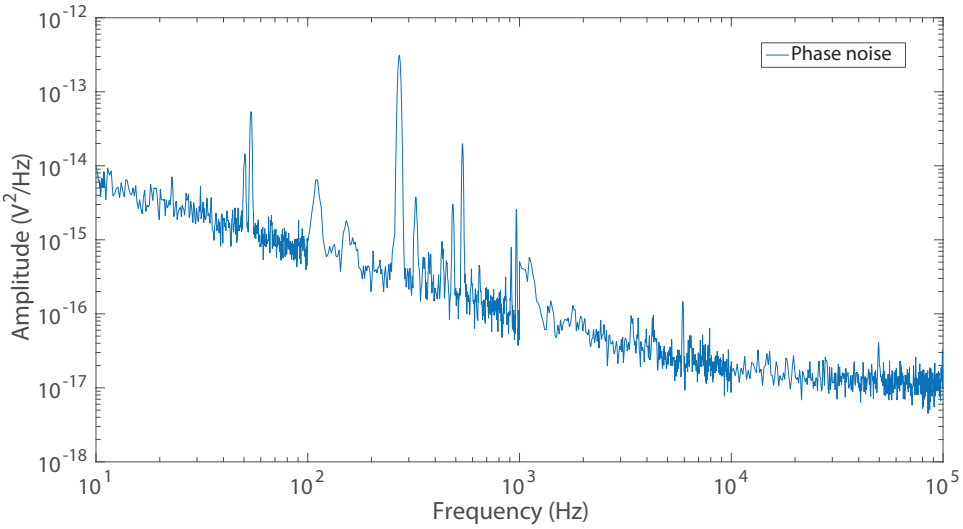

Figure 4.3: The curve shows the power spectral density of the two DDS boards measured using the setup shown in figure 4.1, before the reference is subtracted.

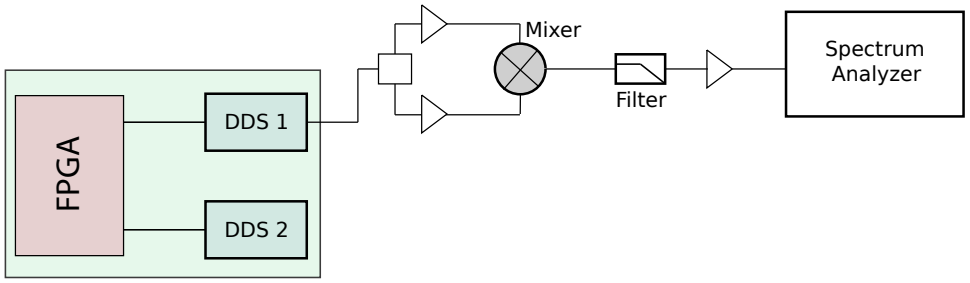

Figure 4.4: Setup for measuring the noise contribution from amplifiers. Here one signal is split in two and sent to the mixer. The phase noise measured only corresponds to phase noise contributed from other components in the setup.

measurement is shown in figure 4.5 alongside of the power spectral density of the DDS phase noise.

The spectrum analyzer measures the signal power per Hz at an offset frequency. This can be converted to the rms voltage per $\sqrt{\text{Hz}}$ at an offset frequency. The rms voltage value of the the phase noise contributions of only the two DDS boards is given by:

$$V_{\text{rms},\Delta\phi_{\text{cleaned}}} = \sqrt{V^2_{\text{rms},\Delta\phi} - V^2_{\text{rms},ref}}, \tag{4.8}$$

where, $V_{\text{rms},\Delta\phi}$ is the noise measurement from the two DDS boards (inclusive of the contributions from amplifiers) and $V_{\text{rms},ref}$ is the measurement from the reference measurment shown in figrue 4.4.

Once the contribution only from the two DDS boards is obtained, we want to calculate the phase noise of one DDS board. Since the noise intrinsic to each DDS board is uncorrelated, it is assumed that they contribute equally [61]. The rms voltage for the phase

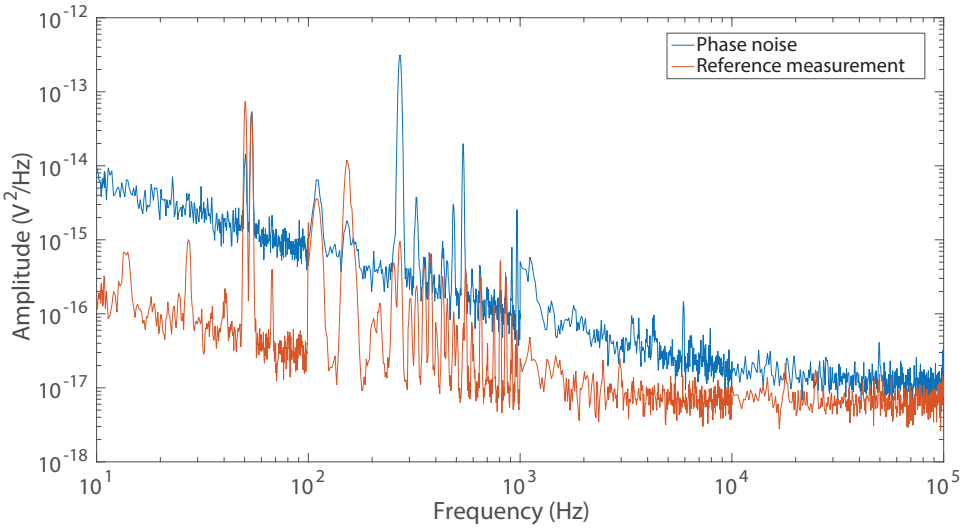

Figure 4.5: The curve on top shows the power spectral density of the phase noise measured using the setup shown in figure 4.1, before subtracting the reference. The bottom curve is the power spectral density of the reference measurement that originates from noise produced by the amplifiers shown in figure 4.4. The power measured in the reference setup needs to be subtracted to get the phase noise contribution of the DDS boards.

noise form one DDS is then given by:

$$V_{\mathrm{rms},DDS} = \sqrt{\frac{V^2_{\mathrm{rms},\Delta\phi_{\mathrm{cleaned}}}}{2}} \tag{4.9}$$

The phase spectral density at some offset frequency f is:

$$S_\phi(f) = \left[\frac{V_{\mathrm{rms},DDS}}{K_\phi}\right]^2 \quad \mathrm{rad}^2/\mathrm{Hz}, \tag{4.10}$$

where K_ϕ the mixer constant introduced earlier. In order to calculate the mean squared phase noise ϕ^2 in a certain bandwidth between frequency f_1 and f_2, one has to integrate the phase spectral density:

$$\phi^2 = \int_{f_1}^{f_2} S_\phi(f) df \tag{4.11}$$

Figure 4.5 shows $V^2_{rms,\Delta\phi}$ and $V^2_{rms,ref}$ for a carrier frequency of 123 MHz from the two DDS boards. Spurious peaks are noticed in both the reference measurement and the phase noise measurement of the two boards. These have to be investigated further. Once the reference measurement is taken, the phase noise from one DDS board can be calculated. The phase jitter in the frequency range from 10 Hz to 1 MHz is calculated to be $9.42{\cdot}10^{-4}$degrees.

To confirm that both the reference and DDS noise measurements were above the pre-

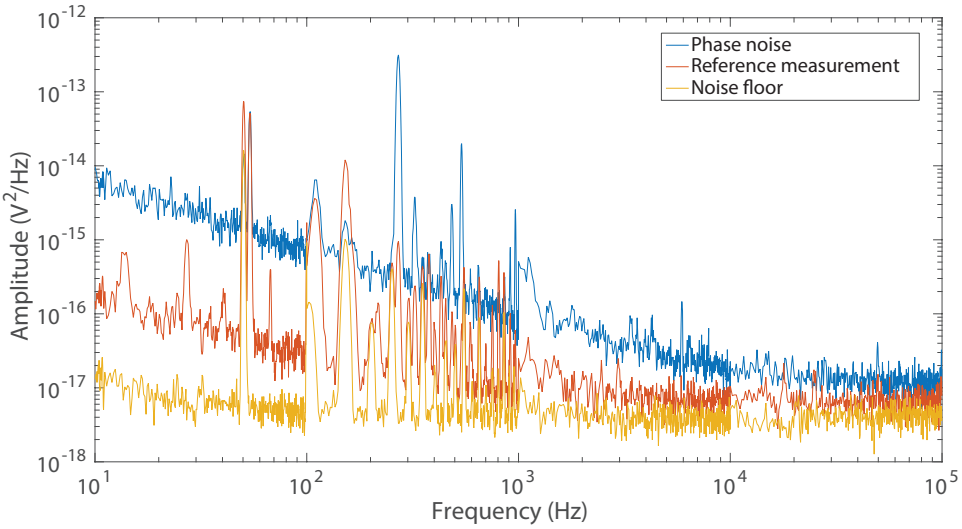

Figure 4.6: This figure shows the noise floor of our measurement setup in comparison to the phase noise measured and the reference measurement.

amplifier noise floor, the power spectral density of the noise floor was measured at the gain setting of 50,000. This is shown in figure 4.6. The offset frequency of interest here is around 100 kHz, corresponding to the trap frequency of the optical lattices. From the plot we can infer that we are working at the limit with this measurement technique since any device with phase noise below the noise floor can not be characterized. Hence, for future phase noise measurements, we will implement the cross-correlation technique [62, 63] where the uncorrelated noise from the amplifiers can be deducted.

The RF frequency of 123 MHz was chosen as the carrier frequency for the phase noise measurement since the data sheet provides a phase noise profile of the AD9915 DDS chip at that frequency. The comparison of the data sheet values with the phase noise from the digital frequency synthesizer are shown in figure 4.7. Comparing with the data sheet values, we see that the phase noise measured is in close agreement with what is expected from the DDS chip's specifications. The phase noise that has been measured is not only of the one originating from a single DDS chip but it also includes the contributions from the FPGA inside the versatile digital frequency synthesizer box. As discussed in section 2.5, a lower phase noise corresponds to a lower heating rate of the atoms. For the new phase noise profile, which is around 18 dB lower than the phase noise of the AD9954 chip, we expect a suppression of heating by two orders of magnitude. This is the theoretical prediction, but in reality, we expect an improvement by one order of magnitude since there are other effects in the experiment, such as intensity fluctuations, that lead to heating of the atoms.

This phase noise has been measured with the frequency fixed at 123 MHz by programming the registers. Since the DDS operates at 80 MHz in the experiment, the phase noise at this carrier frequency was also measured, see appendix A.1. Furthermore, in the experiment the phase modulation of the DDS will always be running. Hence, there is a possibility that the phase noise of the DDS increases when it receives new phase word

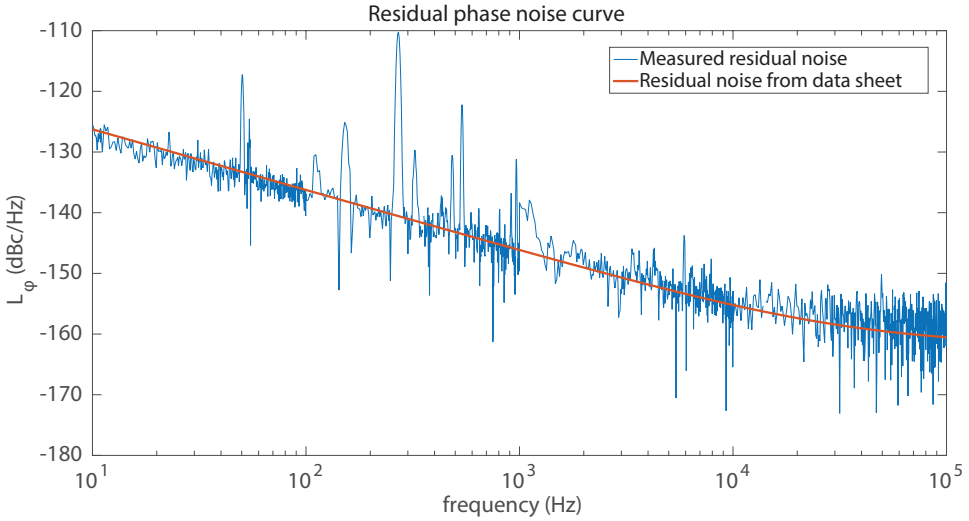

Figure 4.7: The residual phase noise from one output of the versatile digital frequency synthesizer is plotted against the residual phase noise of the AD9915 DDS chip. The carrier frequency is 123 MHz.

data on every clock cycle. The next step is to repeat the phase noise measurement with phase modulation enabled, which however, goes beyond the scope of this master thesis.

Parallel data modulation with test setup

As stated in section 2.6, the AD9915 DDS chip receives data over a parallel port at a frequency of around 150 MHz in comparison to the AD954 DDS chip which is programmed using a serial interface. Regarding parallel data transfer from the FPGA, I have so far tested the parallel capabilities in terms of programming the registers of the three DDS boards. Furthermore, streaming data from the SRAM of the FPGA has also been tested using the SignalTap debugging tool discussed in section 3.2. Before building the versatile digital frequency synthesizer, a test setup was constructed using a different FPGA board (DE2-Nano) and a different DDS chip (AD9910). The AD9910 DDS chip works at a sampling clock of 1 GHz and it also has a parallel data port for phase,frequency and amplitude modulation but a slightly higher phase noise than AD9915. The setup for measuring the phase ramp of the test setup is shown in figure 4.8.

The FPGA was programmed to transfer phase point data in parallel from its on-chip memory after an external trigger. The phase of the AD9910 output was compared to a fixed reference signal from a waveform generator using a PFD[2]. Both the DDS sampling clock and the waveform generator were locked to a 10 MHz reference clock. The phase ramp measured on the oscilloscope is shown in figure 4.9. The output of the PFD is not smooth as expected. This could be due to the DDS or other components in the measurement setup. Since this test setup was just a demonstration of parallel data modulation, the noise was not investigated further.

[2] designed by Professor Marco Prevedelli, based on the MC100EP140 chip

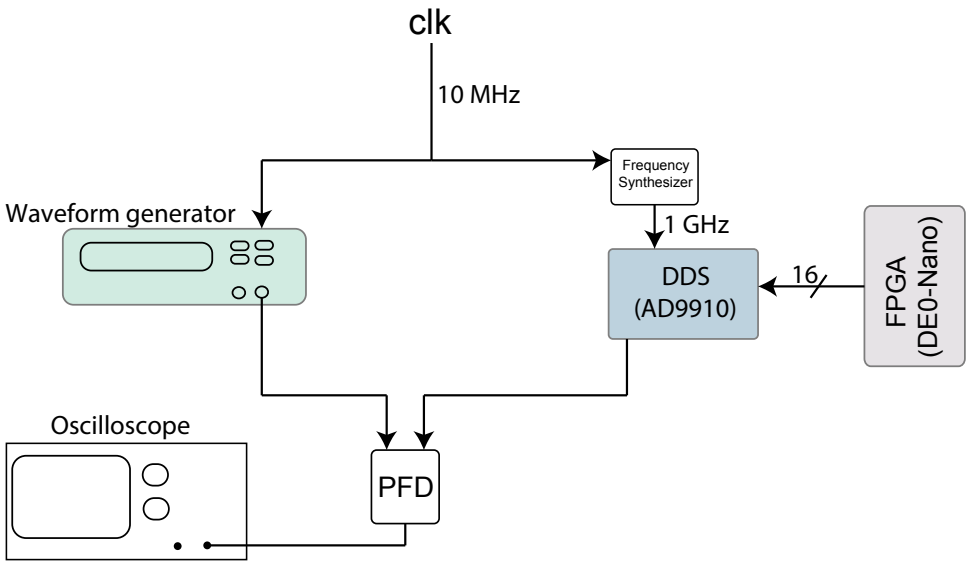

Figure 4.8: Setup for measuring the phase ramp generated by the test setup. The phase ramp of the DDS output is compared with a stable signal from a waveform generator, using a phase frequency discriminator.

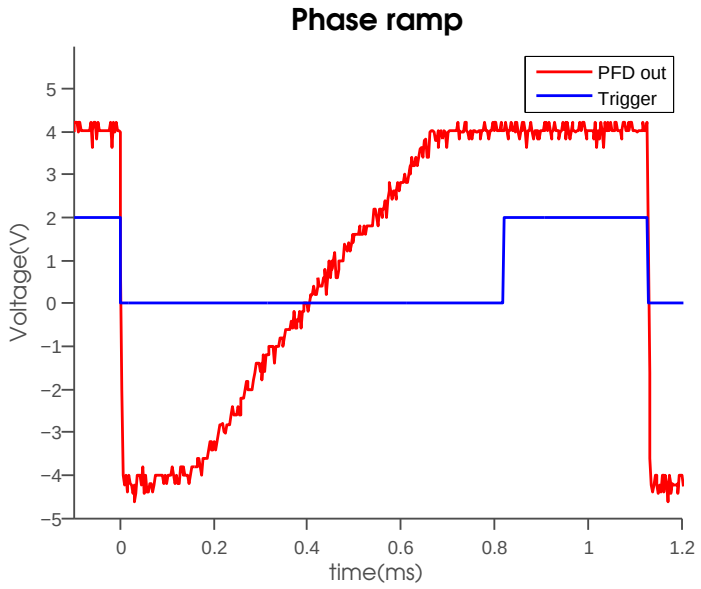

Figure 4.9: Phase ramp gerated by a test setup consisting of a DE0-Nano FPGA board interfaced with an AD9910 DDS chip.

5

Summary and outlook

In this thesis, I have presented a versatile digital frequency synthesizer which I developed based on a field-programmable gate array programming, through a fast communication interface, three direct digital synthesizer. This device will replace the current digital synthesizers which are interfaced with a micro-controller. I programmed the FPGA chip in Verilog, a hardware description language, to interface it with external devices and I implemented a soft-core processor on the FPGA and programmed it in C, a software programming language, in order to handle data flow that is not time-critical.

I have presented the advantages of the new FPGA based synthesizer over the current system, namely, in terms of flexibility and phase noise tabulated in table 5.1. A new low noise DDS chip, the AD9915 from Analog Devices, was chosen to replace the current digital synthesizer in use. From the specifications provided by the company, the new chip has a 20 dB lower phase noise at an offset frequency of 100 kHz. The phase noise of the versatile digital frequency synthesizer was measured to be in close confirmation with the data sheet specifications. Ideally, this corresponds to an improvement in the lifetime of atoms by two orders of magnitude.

Furthermore, the phase of the DDS output can be modulated in real time by an external device, over a parallel data port. The FPGA is used to modulate the phase by sending the digital phase points to the DDS in real time. Compared to the current system, where only 1000 phase points can be stored and used for phase modulation, the new versatile digital frequency synthesizer permits us to store four orders of magnitude higher number of phase points for modulation.

Outlook

The next steps to be performed are testing out the arbitrary phase ramp capabilities of the device. This is the main feature we want in our experiment to perform arbitrary transport sequences. The phase noise of the device should be measured when operating in the streaming mode, where data bits are being transferred to the DDS in real time. Once these test on the versatile digital frequency synthesizer are completed, it will be installed in next months in the experiment and tested for whether it meets our expectations in terms of transport fidelity and lifetime of atoms.

The long term goals of this project include any experiment that would involve long transport distances, but in particular we are interested in realizing an atom interferometer

Previous system (AD9954)	**New system based on a versatile digital frequency synthesizer (FPGA+AD9915)**
1000 data points shared between 4 sequences	Over 10^6 data points shared between 100 sequemces
Phase noise limits the lifetime of atoms	Around 18 dB lower phase noise at 100 kHz
Lifetime in the dark: 5s	Expected lifetime improvement by an order of magnitude

Table 5.1: Advantages of the versatile digital frequency synthesizer over the previous system.

with a large space-time area. The digital atom interferometer implemented previously has been discussed in section 1.1. An improvement over that setup is already in place with the novel polarization synthesis scheme. With the versatile digital frequency synthesizer, we will be able to implement complex arbitrary transport sequences and coherently transport the two arms of the atom interferometer over long distances (on a mm scale). Transport ramps for such mesoscopic splitting of the atomic wave-function will be designed using optimal control theory. Optimal control has been used for transport of trapped atoms [64] and ions [65].

Another application of the arbitrary waveform generation capabilities of the synthesizer is for the state detection technique. Presently, to determine which spin state the atom is in, we use the push-out technique [66] where a push out laser ejects one spin species out of the trap. This destructive state detection technique can be replaced by using long transport ramps to move one spin species out of the field of interest. These atoms can be transported back into the field of view after imaging one spin species. This non-destructive method of state detection has many advantages and has been demonstrated in this group by shifting one spin species over 5 lattice sites for an ideal negative measurement [45].

6

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During the course of my thesis work, I have had the pleasure of working with a number of wonderful people from whom I have learned a lot about this fascinating field of physics and who have continuously supported me during the course of my work. First and foremost, I would like to thank Professor Meschede for introducing me to the exciting developments in the field of quantum optics in his lectures and then letting me join his research group for my thesis work. I would also like to thank Professor Weitz for kindly agreeing to be my second supervisor.

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A

Appendix

A.1 Phase noise at 80 MHz

The measurement results shown in chapter 4 are taken at a carrier frequency of 123 MHz. This was done in order to compare the noise profile with the data sheet. In the experiment, the AOM is driven at a frequency of 80 MHz. Hence the versatile digital frequency synthesizer will be generating a frequency at 80 MHz. The phase noise at this frequency was tested and is shown in figure A.1. The phase noise at 80 MHz suffers from many spurious peaks. The cause of these spurious peaks has to be investigated. Since these peaks were not observed for other frequencies, we will have to scan the carrier frequency of the DDS around 80 MHz in order to find the optimum frequency where the spurious peak contribution is suppressed.

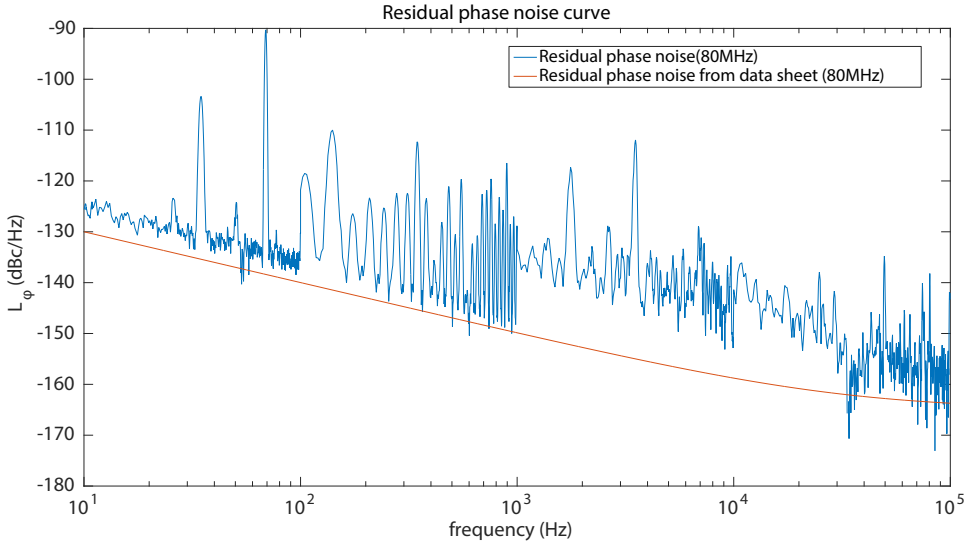

Figure A.1: Residual phase noise of versatile digital frequency synthesizer at 80 MHz. The phase noise from the data sheet is extracted for comparison.

A.2 Modeling phase noise for the AD9954 and AD9915

The phase noise model has been explained in section 2.6. To residual phase noise of the AD9954 and AD9915 DDS chips were extracted from the data sheet. These were fit with the model for the phase noise using Matlab®. The phase noise of direct digital synthesizers is [50, 51]:

$$S_{\mathrm{DDS}}(F) = (K_{\mathrm{DDS}})^2\left(\frac{10^{k_2}}{F^2} + \frac{10^{k_1}}{F} + 10^{k_4}\right) + 10^{k_3} + S_q \ , \tag{A.1}$$

where F is the offset frequency, K_{DDS} is the ratio of the output frequency to the clock frequency. k_1,k_2,k_3,k_4 and S_q are the fitting parameters. Figures A.2 and A.3 show the fits for AD9954 and AD9915 respectively.

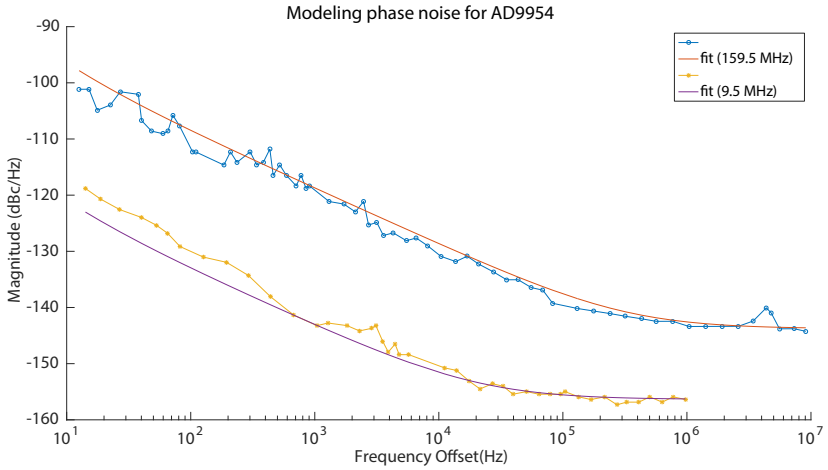

Figure A.2: Fitting phase noise data for AD9954 with equation A.1.

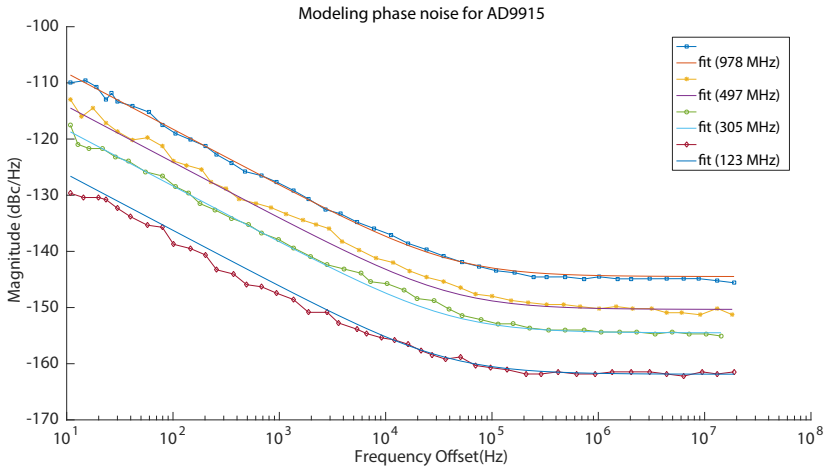

Figure A.3: Fitting phase noise data for AD9915 with equation A.1.

A

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Acronyms

AOM acousto-optic modulator. 12, 13, 16, 17, 20, 23, 51

DAC digital to analog convertor. 15

DDS direct digital synthesizer. 13–28, 30, 32–34, 37–45, 47, 51, 52, 59, 60

FIFO first-in, first-out. 32

FPGA field-Programmable gate array. 20, 23–29, 31–35, 43–45, 47, 59, 60

HSMC high speed mezannine card. 28, 30

LUT look-up table. 24

MAC media access control. 32

MOT magneto optical trap. 12

OPLL optical phase locked loop. 13

PBS polarizing beamsplitter. 12, 13

PFD phase-frequency discriminator. 13, 44

PID proportionl-integral-derivative. 13

PLL phase lock loop. 31

RAM random access memory. 24

SDC synopsys design contraints. 34, 35

SDRAM synchronous dynamic random access memory. 26–28, 30, 32

SRAM static random-access memory. 20, 27, 28, 30, 44

TTL transistor-transitor logic. 26, 27

VCO voltage controlled oscillator. 13